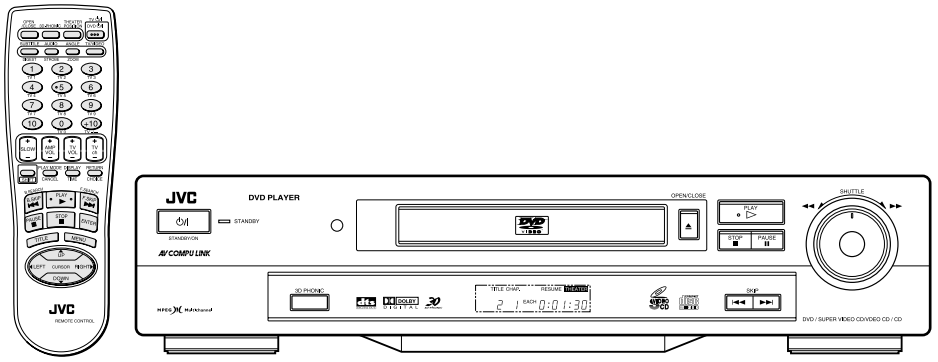
JVC

SERVICE MANUAL

DVD PLAYER

XV-521BK
XV-523GD



Area Suffix
XV-521BK

UF	China
1U	US military
3U	Malaysia,Thailand, Philippine...etc.

Area Suffix
XV-523GD

UB	Hong Kong
UF	China
US	Singapore
2U	Turkey,South Africa, Egypt...etc.
3U	Malaysia,Thailand, Philippine...etc.
4U	Brazil,Mexico,Peru...etc.

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No.20869
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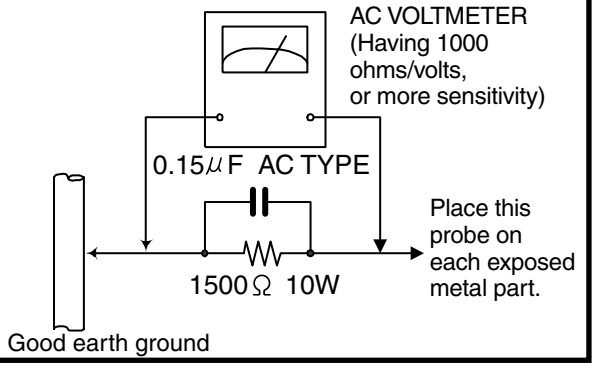
Safety precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer`s warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage currnet check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.
   - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet , particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.)
   - Alternate check method
     Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
     Measure the AC voltage across the resistor with the AC voltmeter.
     Move the resistor connection to eachexposed metal part, particularly any exposed metal part having a return path to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ ***CAUTION*** **Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.**

Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

1.1. Grounding to prevent damage by static electricity

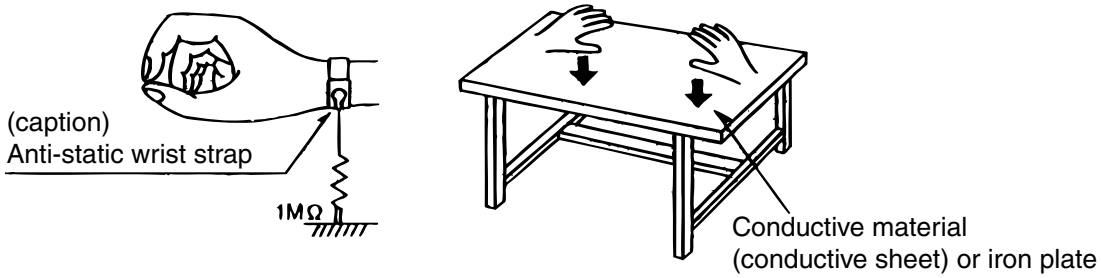
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

1.1.1. Ground the workbench

1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

1.1.2. Ground yourself

1. Use an anti-static wrist strap to release any static electricity built up in your body.



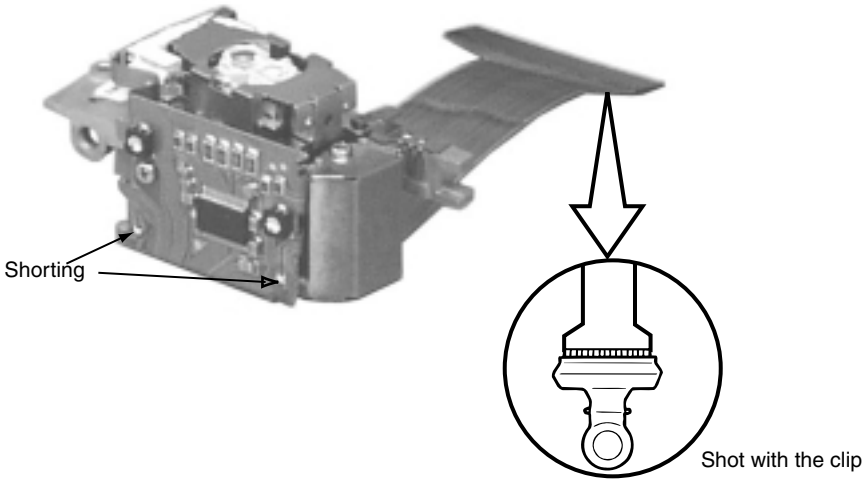
1.1.3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)
2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

1.2. Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.
2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.
3. Handle the flexible cable carefully as it may break when subjected to strong force.
4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

- Note : Short the land after shorting the terminal on the flexible cable using a clip, etc., when using an ungrounded soldering iron.
- Note : After shorting the laser diode according to the procedure above, remove the solder according to the text explanation.



Disassembly method

< Main body>

■ Removing the top cover (See Fig.1)

1. Remove the four screws A on both side of the body.
2. Remove the two screws B on the back of the body.
3. Lift up the rear part of the top cover while pulling the lower part of the sides, then detach upward.

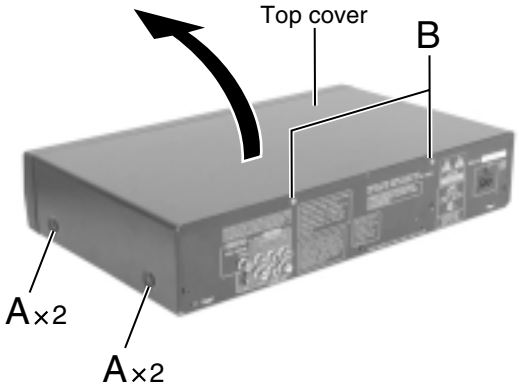


Fig.1

■ Removing the rear panel (See Fig.2)

・Prior to performing the following procedure, remove the top cover.

1. Remove the seven screws C on the back of the body.

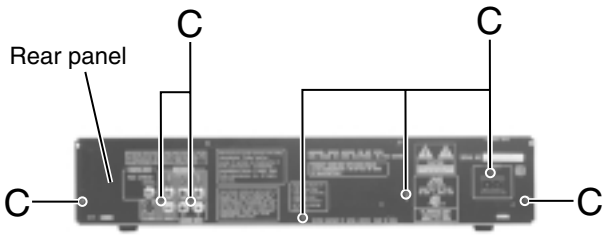


Fig.2

■ Removing the fitting (See Fig.3 to 6)

・Prior to performing the following procedure, remove the top cover.

ATTENTION: To remove the front panel assembly and the DVD mechanism assembly, remove the fitting in advance.

—— by hand ——

1. Turn over the body. Insert a screwdriver into the hole of the bottom chassis and turnit. The loading tray will be ejected out of the front panel assembly.
2. Pull the loading tray toward the front.
3. Remove the fitting upward from the loading tray at the joints b.
4. Push and return the loading tray.

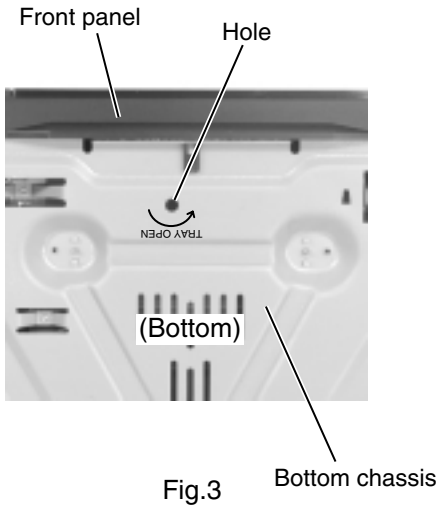


Fig.3

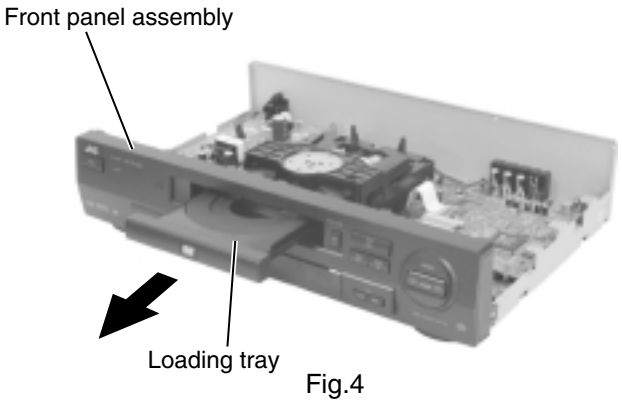


Fig.4

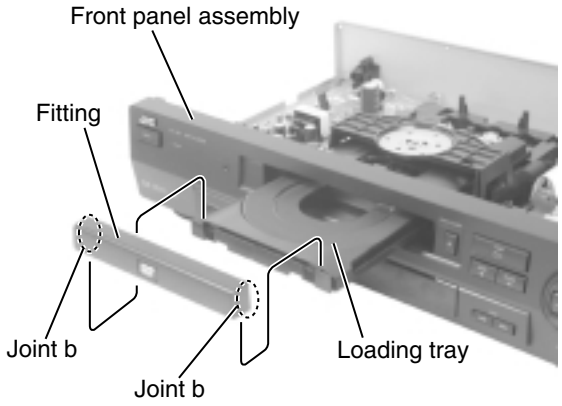


Fig.5

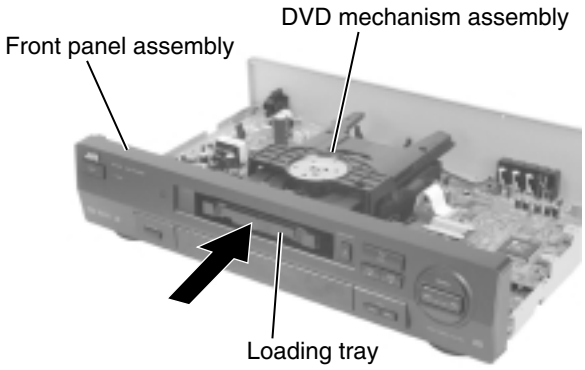


Fig.6

■ Removing the front panel assembly (See Fig.7 to 10)

- Prior to performing the following procedure, remove the top cover and the fitting.

1. Disconnect the card wire from connector CN703 on the main board.
2. Turn over the body and remove the screw D attaching the front panel assembly.
3. Release the five joints c on both sides and bottom of the body and remove the front panel assembly toward the front.

ATTENTION: The connector CN832 on the front panel assembly and CN971 on the AC jack board will be disconnected at the same time.

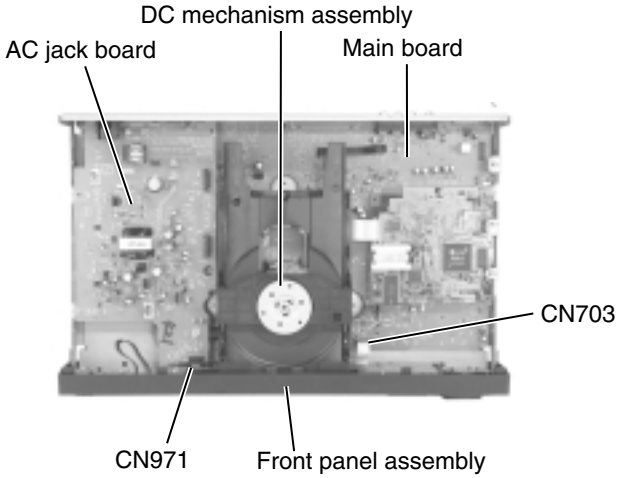


Fig.7

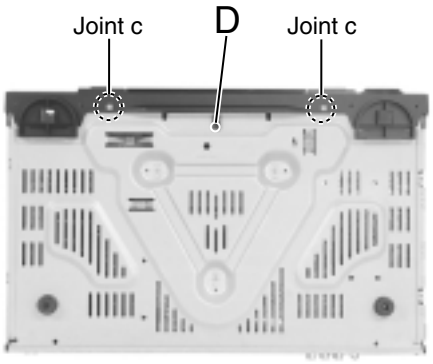


Fig.8

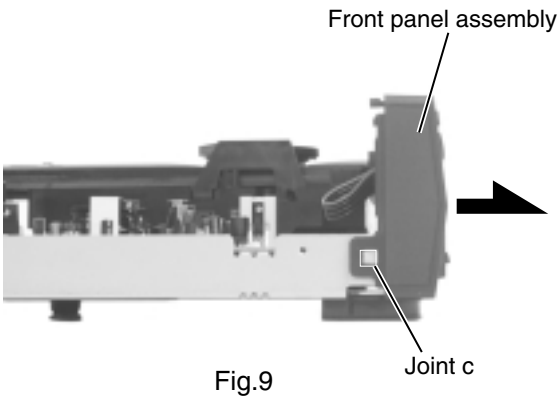


Fig.9

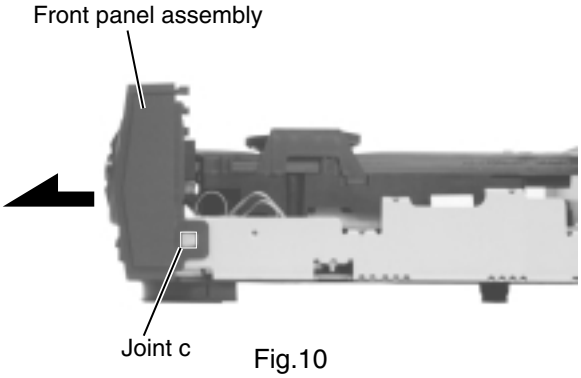


Fig.10

■ Removing the DVD mechanism assembly (See Fig.11 to 14)

・Prior to performing the following procedure, remove the top cover and the front panel assembly.

1. Disconnect the card wire from connector CN101 on the DVD Servo.

2. Disconnect the harness from connector CN031 on the DVD mechanism assembly.

3. Remove the screw E on the rear left part of the loading tray.

3. From the front side of the DVD mechanism assembly, move the lever d in the direction of the arrow and pull out the loading tray.

4. Remove the two screws F on the upper side of the DVD mechanism assembly. Then release the two joints e and detach the clamper base back-upward.

5. Remove the three screws G attaching the DVD mechanism assembly.

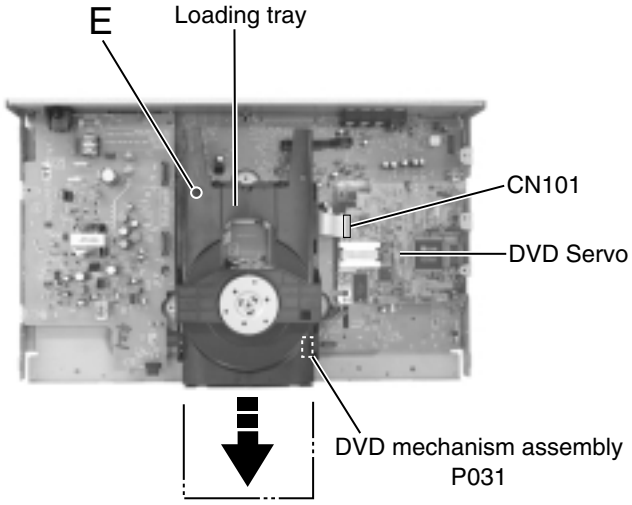


Fig.11

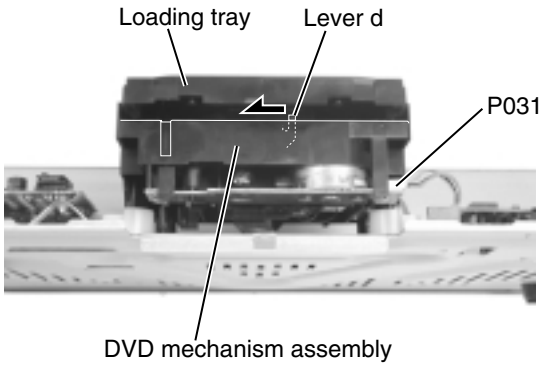


Fig.12

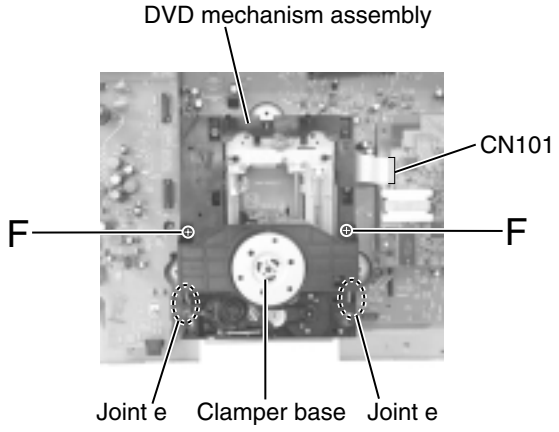


Fig.13

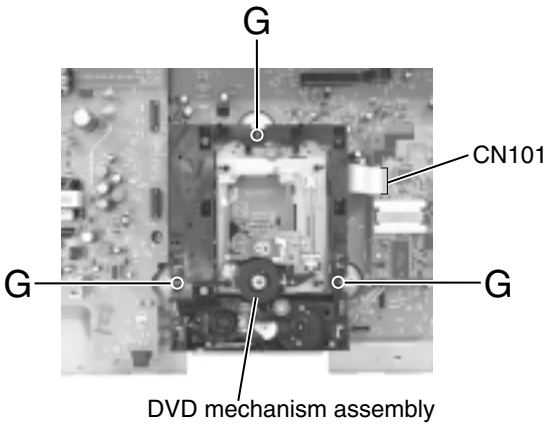


Fig.14

■ Removing the AC jack board (See Fig.15 and 16)

・Prior to performing the following procedure, remove the top cover and the front panel assembly.

1. Remove the two screws H attaching the AC jack board.
2. Remove the two screws C on the rear panel.
3. Disconnect connector CN951 and CN961 on the AC jack board from CN704 and CN705 on the main board respectively.

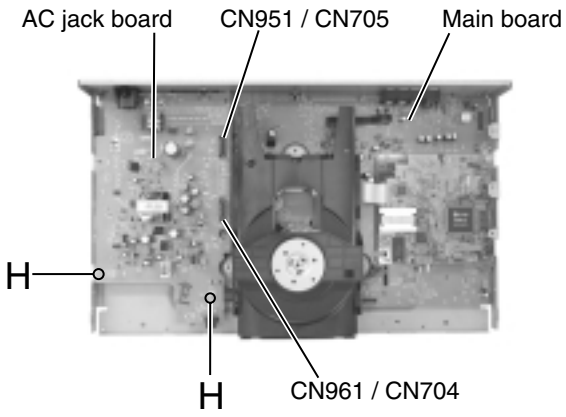


Fig.15

Fig.16

■ Removing the DVD Servo (See Fig.17 and 18)

・Prior to performing the following procedure, remove the top cover.

1. Remove the screw I attaching the DVD Servo.
2. Pull out the DVD Servo from the fix f while pinching the fix f.
3. Disconnect connector CN501, CN502 and CN503 on the DVD Servo from CN601, CN701 and CN706 on the main board respectively.

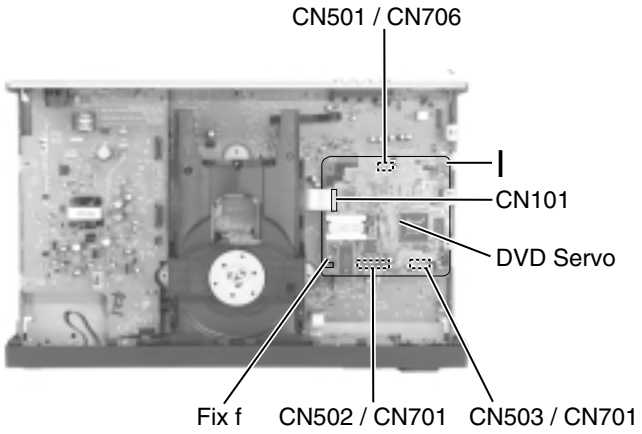
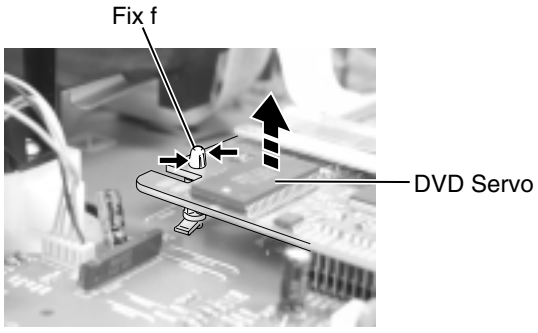


Fig.17



Main board

Fig.18

■ Removing the main board (See Fig.19 and 20)

・Prior to performing the following procedure, remove the top cover, the front panel assembly, the DVD mechanism assembly, the AC jack board and the DVD Servo.

1. Remove the three screws J attaching the main board.
2. Remove the two screws C on the rear panel.

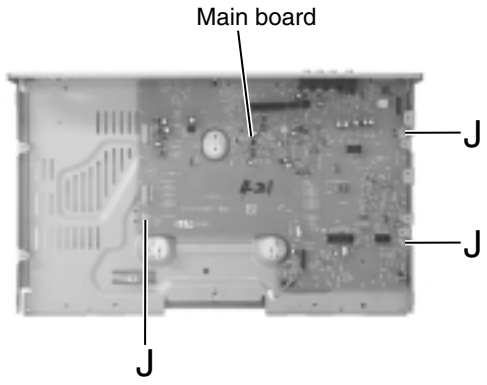


Fig.19

<Front panel assembly>

・Prior to performing the following procedure, remove the top cover and the front panel assembly.

■ Removing the power switch board (See Fig.21)

1. Unsolder connector FW841 on the power switch board on the back of the front panel assembly.
2. Remove the two screws K attaching the power switch board.
3. Push the two tabs g in the direction of the arrow and remove the power switch board.

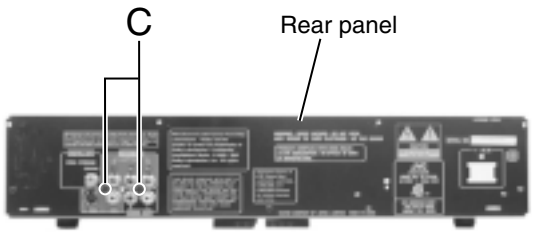


Fig.20

■ Removing the LCD board (See Fig.22)

1. Unsolder connector FW802 and soldering h on the LCD board.
2. Remove the four screws L attaching the LCD board.

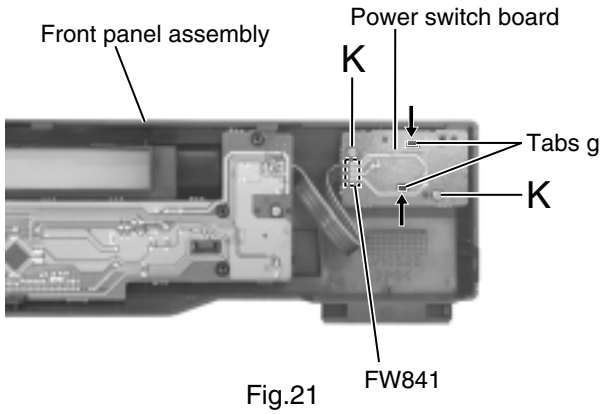


Fig.21

■ Removing the search switch board (See Fig.20)

1. Unsolder soldering i on the search switch board.
2. Remove the three screws M.
3. Release the four tabs j in the direction of the arrow and remove the search switch board.

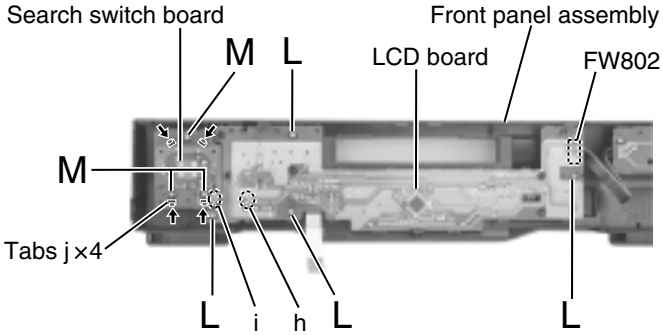


Fig.22

<DVD mechanism>

■ Removing the traverse mechanism unit (See Fig.1 and 2)

1. Remove the screw A and the spring on the upper side of the loading base assembly.

2. Move the rear part of the traverse mechanism unit upward and pull backward to release the two joints a with the base chassis.

   ATTENTION: When reattaching, engage the two joints a and make sure the front springs and the four insulators of the traverse mechanism unit are correctly attached.

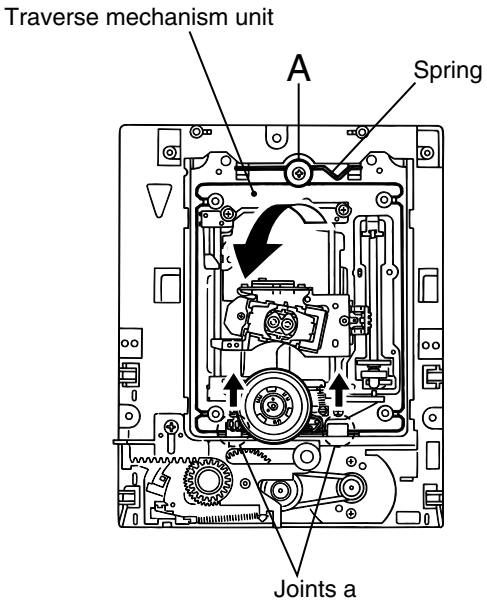


Fig.1

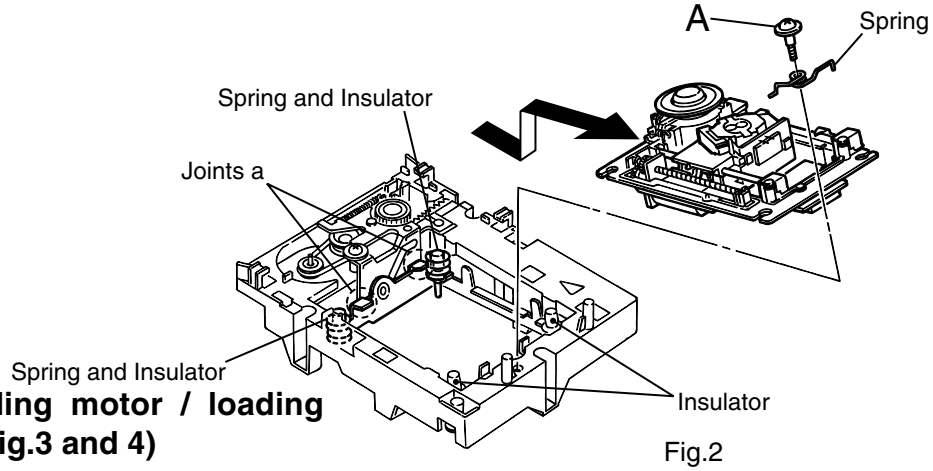


Fig.2

■ Removing the loading motor / loading motor board (See Fig.3 and 4)

1. Move the cam plate on the upper side of the loading base assembly in the direction of the arrow.

2. Remove the belt from the motor pulley.

3. Remove the two screws B attaching the loading motor.

4. Turn over the loading base assembly and release the loading motor board from the three tabs b while spreading them outward. The loading motor board will be detached with the loading motor.

5. Unsolder soldering c on the loading motor board and remove the loading motor.

   Ref.: To remove the loading motor board only, unsolder soldering c on the loading motor and release the three tabs b.

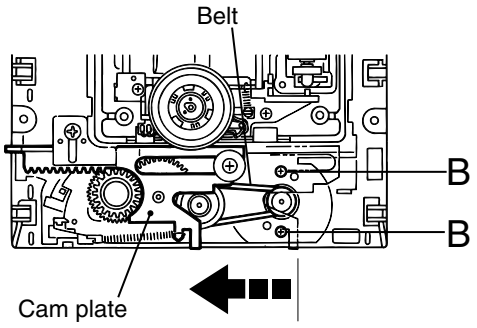


Fig.3

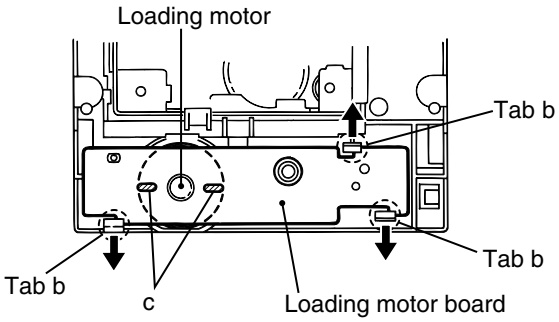


Fig.4

■Removing the pickup (See Fig.5 to 9)

※It is not necessary to remove the traverse mechanism unit.

1. Solder soldering d on the flexible board next to the pickup unit.

2. From the bottom of the traverse mechanism unit, disconnect the flexible wire from CN10 on the pickup board.

   ATTENTION: Disconnecting the flexible wire without soldering may cause damage to the pickup.

3. Remove the screw C attaching the shaft stopper (R) on the upper side of the traverse mechanism unit. Pull the side of the shaft stopper (R) outward to release the joint e and remove it upward. Remove the skew spring at the same time.

4. Move the shaft in the direction of the arrow to release it from the part f.

5. Release the joint g with the shaft and remove the pickup with the shaft.

6. Pull out the shaft.

7. Remove the screw D attaching the switch actuator.

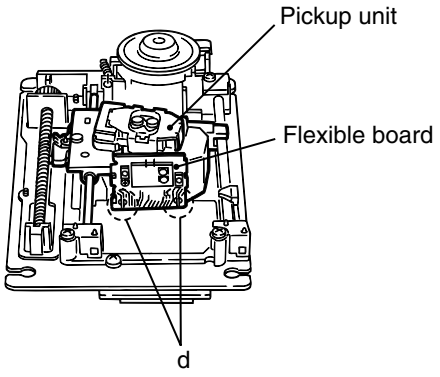


Fig.5

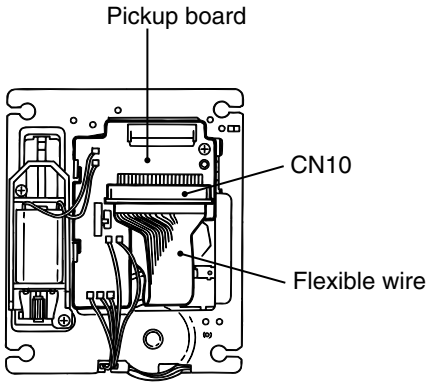


Fig.6

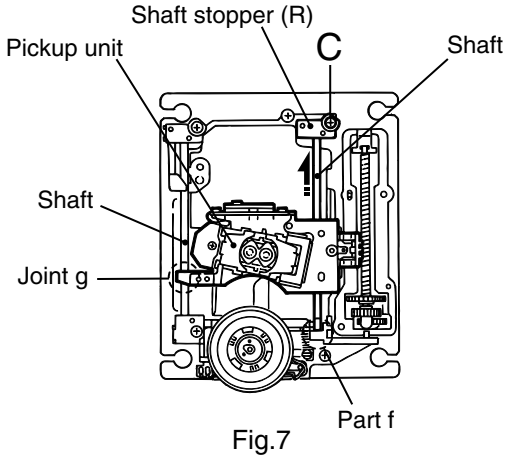


Fig.7

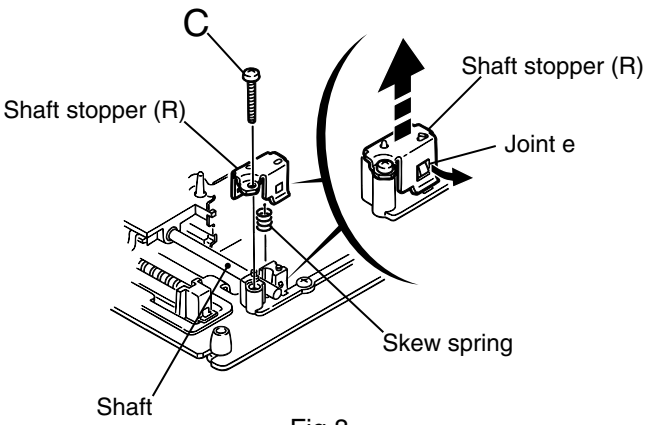


Fig.8

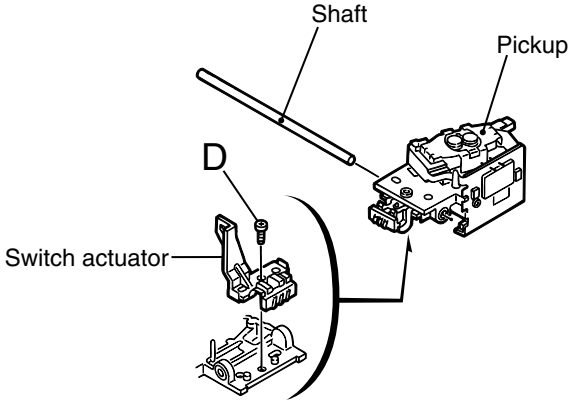


Fig.9

■ Removing the pickup board (See Fig.5 and 10)

※ It is not necessary to remove the traverse mechanism unit.

1. Solder soldering d on the flexible board next to the pickup unit.
2. From the bottom of the traverse mechanism unit, disconnect the flexible wire from CN10 on the pickup board.

   ATTENTION: Disconnecting the flexible wire without soldering may cause damage to the pickup.
3. Unsolder soldering h, i and j of each harness on the pickup board.
4. Remove the screw E attaching the pickup board and release the two joints k.

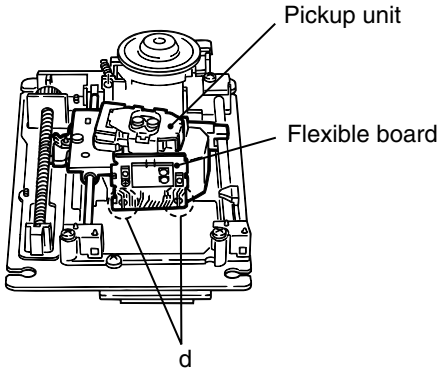


Fig.5

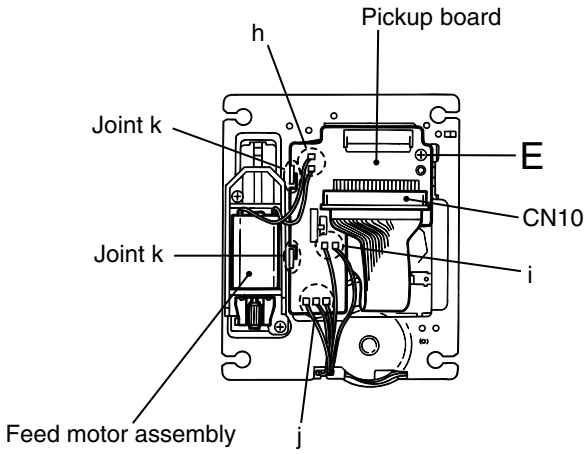


Fig.10

■ Removing the feed motor assembly (See Fig.5, 10 and 11)

・ Prior to performing the following procedure, remove the traverse mechanism unit.

1. Solder soldering d on the flexible board next to the pickup unit.
2. From the bottom of the traverse mechanism unit, disconnect the flexible wire from CN10 on the pickup board.

   ATTENTION: Disconnecting the flexible wire without soldering may cause damage to the pickup.
3. Unsolder soldering h of the motor harness on the pickup board.
4. Remove the two screws F attaching the feed motor assembly and remove the thrust spring. Move the feed motor assembly in the direction of the arrow to pull it out from the feed holder.

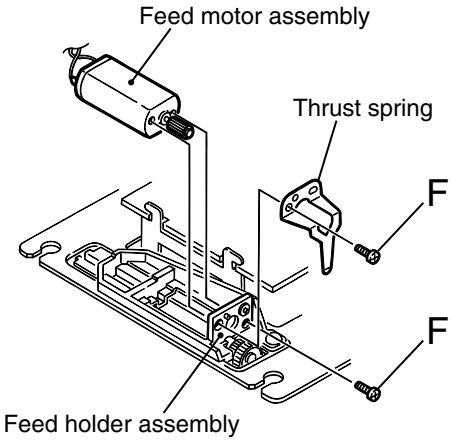


Fig.11

■Removing the turn table assembly (See Fig.5, 10, 12 and 13)

- Prior to performing the following procedure, remove the traverse mechanism unit.

1. Solder soldering d on the flexible board next to the pickup unit.

2. From the bottom of the traverse mechanism unit, disconnect the flexible wire from CN10 on the pickup board.

   ATTENTION: Disconnecting the flexible wire without soldering may cause damage to the pickup.

3. Unsolder soldering i and j of the harness extending from the turning table assembly to the pickup board.

4. Remove the screw G attaching the shaft stopper (F) on the upper side of the traverse mechanism unit. Pull the side of the shaft stopper (F) outward to release the joint l and remove it upward. Remove the spring at the same time.

5. Remove the screw H attaching the turn table assembly.

6. Move the turn table assembly outward and pull out from the shaft. Then remove it from the base chassis.

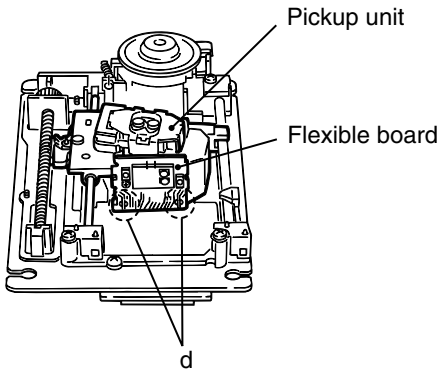


Fig.5

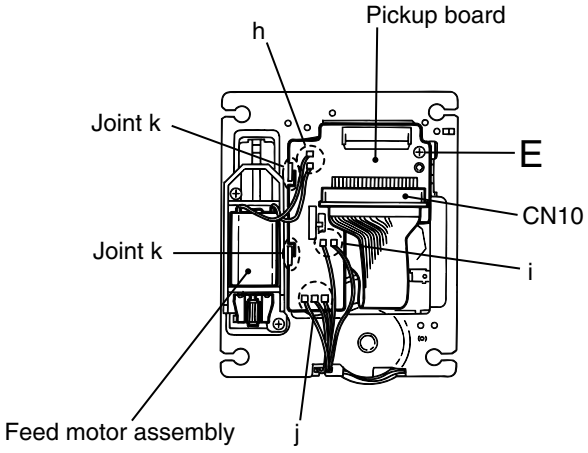


Fig.10

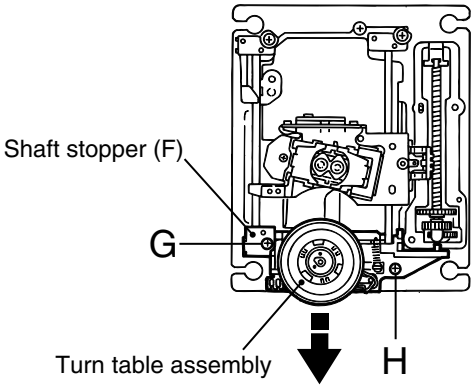


Fig.12

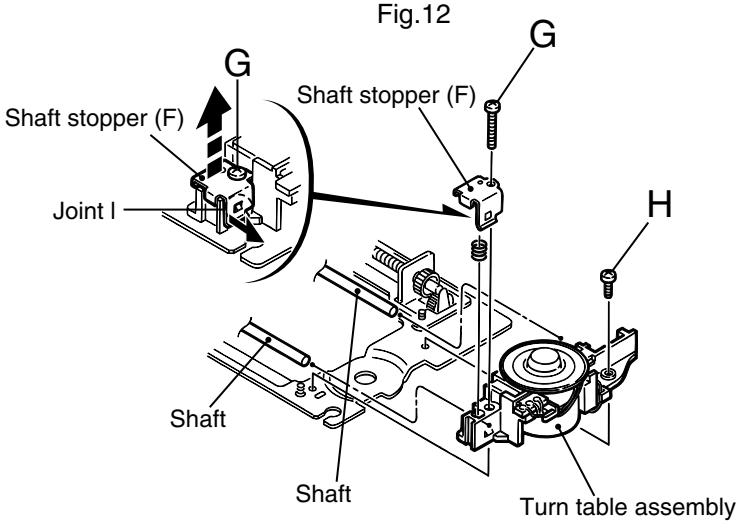


Fig.13

Main adjustment

Adjustment and confirmation matter

(1) Auto adjustment method

If microprocessor (IC401, IC402, IC791, IC403) or Pick-up is replaced, initialize the DVD player in the following matter:

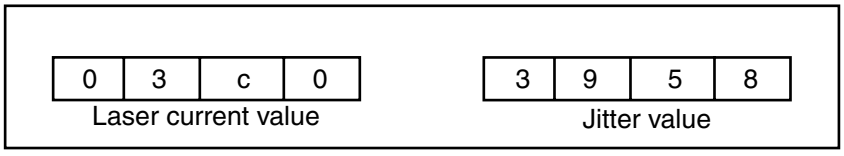
1. Initialize the DVD player in the following matter:

1) Make sure that no disc is on the tray.
2)Insert the power pulag to the outret while pressing "PLAY" and "OPEN/CLOSE" button at the same time.
FL Display indicate "TEST＊＊￥" (＊＊;Version. ￥;Region code)
3)Press 3D-PHONIC button. And EEPROM initialize start.
4)When indicate "V.REPLACE" on the display , initialize finished.

＊ The test mode is cancelled when the power is turned off.

(2)Flap adjustment of the Pick-up guide shaft

1) Make sure that no disc is on the tray.
2)Insert the power pulag to the outret while pressing "PLAY" and "OPEN/CLOSE" button at the same time.
FL Display indicate "TEST＊＊￥" (＊＊;Version. ￥;Region code)
3)Press the "OPEN/CLOSE" button to move the tray outward.
Put the Test Disc (VT-501)on the tray and press "OPEN/CLOSE" button.
The tray should move inward (Note:Don't push to close the tray directly by hand etc.
4)Press the "PLAY" button.
5)The laser current and the jitter value is displayed on the FL indicator as follows.



FL indicator

6)Set the Jitter value of FL indicator to minimum by adjusting the pick-up guide shaft flap.

＊ The test mode is cancelled when the power is turned off.

Table for FL conversion value

1. Electric current

FL display	Electric Current (mA)	Result	FL display	Electric Current/Result	
000c,000b	25	OK	03cA	59	OK
000A	26	OK	03c9,03c8	60	OK
0009,0008	27	OK	03c7,03c6	61	OK
0007,0006	28	OK	03c5,03c4	62	OK
0005,0004	29	OK	03c3,03c2	63	OK
0003,0002	30	OK	03c1,03c0	64	OK
0001,0000	31	OK	03bF,03bE	65	NG
03FF,03FE	32	OK	03bd,03bc	66	NG
03Fd,03Fc	33	OK	03bb,03bA	67	NG
03Fb,03FA	34	OK	03b9,03b8	68	NG
03F9,03F8	35	OK	03b7,03b6	69	NG
03F7,03F6	36	OK	03b5,03b4	70	NG
03F5,03F4	37	OK	03b3,03b2	71	NG
03F3,03F2	38	OK	03b1,03b0	72	NG
03F1,03F0	39	OK	03AF,03AE	73	NG
03EF,03EE	40	OK	03Ad,03Ac	74	NG
03Ed,03Ec	41	OK	03Ab,03AA	75	NG
03Eb,03EA	42	OK	03A9	76	NG
03E9	43	OK	03A8,03A7	77	NG
03E8,03E7	44	OK	03A6,03A5	78	NG
03E6,03E5	45	OK	03A4,03A3	79	NG
03E4,03E3	46	OK	03A2,03A1	80	NG
03E2,03E1	47	OK	03A0,039F	81	NG
03E0,03dF	48	OK	039E,039d	82	NG
03dE,03dd	49	OK	039c,039b	83	NG
03dc,03db	50	OK	039A,0399	84	NG
03dA,03d9	51	OK	0398,0397	85	NG
03d8,03d7	52	OK	0396,0395	86	NG
03d6,03d5	53	OK	0394,0393	87	NG
03d4,03d3	54	OK	0392,0391	88	NG
03d2,03d1	55	OK	0390,038F	89	NG
03d0,03cF	56	OK	038E,038d	90	NG
03cE,03cd	57	OK	038c,038b	91	NG
03cc,03cb	58	OK			

2. Jitter value

FL display	Conversion value (%)	FL display	Conversion value (%)
3818	4.7	3b18	10.5
3828	4.8	3b28	10.6
3838	4.9	3b38	10.7
3848	5.1	3b48	10.8
3858	5.2	3b58	10.9
3868	5.3	3b68	11.1
3878	5.4	3b78	11.2
3888	5.5	3b88	11.3
3898	5.7	3b98	11.4
38A8	5.8	3bA8	11.5
38b8	5.9	3bb8	11.7
38c8	6.0	3bc8	11.8
38d8	6.1	3bd8	11.9
38E8	6.3	3bE8	12.0
38F8	6.4	3bF8	12.1
3918	6.6	3c18	12.4
3928	6.7	3c28	12.5
3938	6.9	3c38	12.7
3948	7.0	3c48	12.7
3958	7.1	3c58	12.9
3968	7.2	3c68	13.0
3978	7.3	3c78	13.1
3988	7.5	3c88	13.2
3998	7.6	3c98	13.3
39A8	7.7	3cA8	13.5
39b8	7.8	3cb8	13.6
39c8	7.9	3cc8	13.7
39d8	8.1	3cd8	13.8
39E8	8.2	3cE8	13.9
39F8	8.3	3cF8	14.1
3A18	8.5	3d18	14.3
3A28	8.7	3d28	14.4
3A38	8.8	3d38	14.5
3A48	8.9	3d48	14.7
3A58	9.0	3d58	14.8
3A68	9.1	3d68	14.9
3A78	9.3	3d78	15.0
3A88	9.4	3d88	15.1
3A98	9.5	3d98	15.3
3AA8	9.6	3dA8	15.4
3Ab8	9.7	3db8	15.5
3Ac8	9.9	3dc8	15.6
3Ad8	10.0	3dd8	15.7
3AE8	10.1	3dE8	15.9
3AF8	10.2	3dF8	16.0

Flap adjustment method

Measurement	Adjustment point	Mode	Disc
FL Display	Refer to Fig.2	Reproduction part	VT-501

Measurement machine	connections	Extension cord No.
No need	Refer to Fig.1	QUQ605-4040AJ
General tool : Hex-head wrench(1.27mm)		

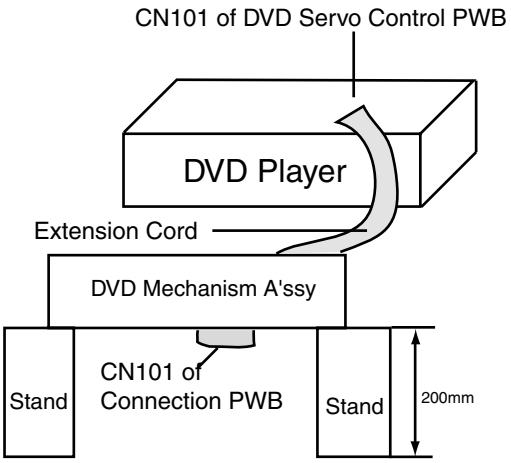


Fig.1

"Flap adjustment" of the Pick-up guide shaft adjusts
"Tangential adjustment machine screw" A and
"Tilt adjustment machine screw" B from the
DVD Mechanism A'ssy bottom.

1. The part at the center on the DVD test disc is reproduced.
2. The flap adjustment screws is turned alternately and set the jitter value of FL indicator to its minimum.

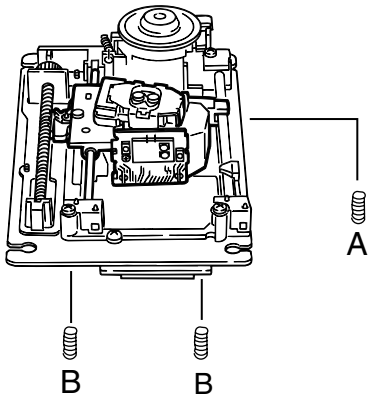


Fig.2

Note

1. The tangential adjustment is done finish and, then, tilt is adjusted.
2. The repeat the adjustment 2-3 times,for best result.
3. The final adjustment should be tilt adjustment.

Confirmation after adjustment.

Confirm to reproduce video CD and CD after the DVD test disc is adjusted and to find abnormality.

(3) About keeping the disc

As for the DVD test disc, plane accuracy is demanded.Please note the keeping place on the disc.

1. Please do not put the disc directly on the work desk etc. after uses .
2. To keep the planarity of the disc, politely handle ,and please put in a special case and keep the disc vertically after uses .
   Please keep keeping the disc in a cool place where direct sunshine and the air-conditioning wind do not drive.
3. When the disc curves,an accurate adjustment cannot be done.
   Please exchange for a new test disc and adjust optics.
4. Other discs might not be able to be reproduced when adjusting on a curved disc.

Point of adjustment

* Please execute the static electricity protection measures before starting the adjustment.
* When the following parts are exchanged,optical adjustment "Adjust the flap of Pick-up guide shaft" is necessary.
  1. The disc motor was exchanged.
  2. The laser pick up was exchanged.
  3. The traverse motor unit was exchanged.

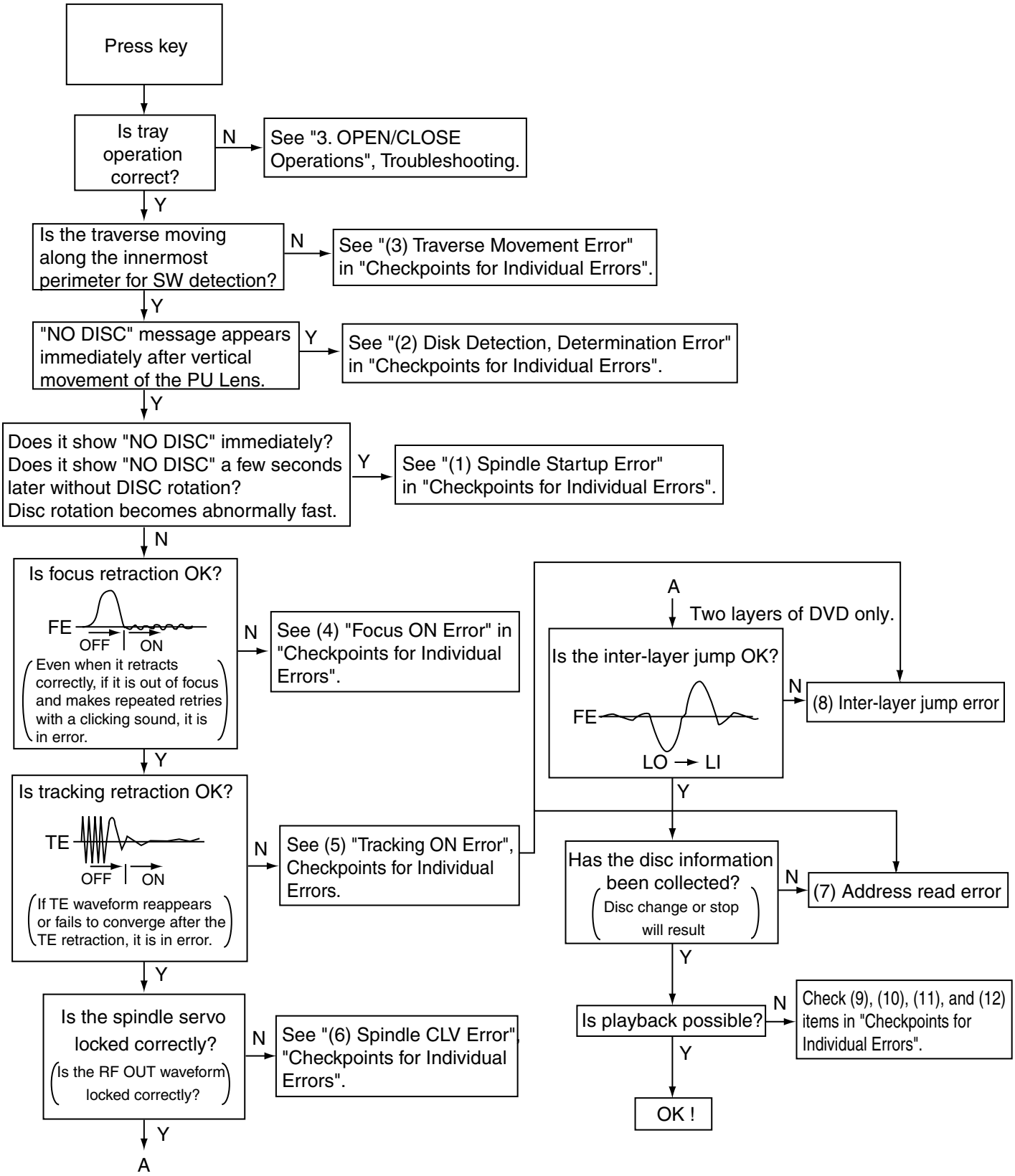
Note

Additionally, please adjust the flap of the disc motor when the picture quality deterioration is seen .The basic adjustment though, is unnecessary for part exchange in the traverse.
An optical adjustment in the laser pick up cannot be done.
Please adjust the flap of the disc motor after exchanging the laser pick up.

* When the traverse unit is exchanged, the adjustment is basically unnecessary.

Troubleshooting

Servo volum



Checkpoints for individual errors

(1) Spindle startup error

1. Defective spindle motor
   * Is the resistance between CN101 "34-35" and "36-37" about 10 to 6 ohms? (Measure it with the power OFF.)
   * Is the voltage waveform for the hall element CN101"40" square-wave? (During rotation)
2. Defective spindle driver (IC271)
   * Is DC voltage applied to IC271"14-15"?
   * Is IC271"25" set to "H" (SPMUTE)?
3. Servo IC
   Is control available at the motor driver?
   * IC201"52" → R290 50% duty during stop. Variable during rotation (Fluctuates especially during startup.)
     If no control available: pattern servo IC, IC201.
4. Is FG input in the servo IC?
   * IC271"42" → IC271"41" → 0275 → IC201"53" (FG) FG waveform observation
     If no FG input: pattern IC271, IC201.

(2) Disk detection, distinction error (no discs, no REFNV)

1. Defective laser
2. Defective front-end processor (IC101)
3. Defective APC circuit → Q101, Q102
4. Defective pattern
   A pattern between all CN101 PIC related patterns and the IC101
5. Defective servo IC (IC201)
6. IC101
   Are IC101"20"(AS), IC101"41"(RFENV), and IC101"22"(FE) included in the signal to IC201?

(3) Traverse movement error

1. Defective traverse motor
   * Is voltage applied between CN101 "38" and "39"?
2. Defective BTL driver
   * Is voltage applied on IC271 "9" and "10"?
   * Is MUTE1 terminal "26" of IC271 set to "H"?
   * Is drive voltage applied to servo IC201"51"?
     Defective servo IC or defective pattern

(4) Focus ON error

1. Is FE produced? → Pattern, IC101
2. Is FODRV signal produced? (R280) → Pattern, IC201
3. Is drive voltage available?
   If not available: pattern, driver, or mechanism. (Turn the power OFF then measure the resistance between CN101 "30" and "31".)
4. Defective mechanism

(5) Tracking ON error

1. When tracking loop is not retracted, TE waveform does not converge.
2. Defective mechanism
   The possible cause for unavailability of correct retraction is that automatic adjustment cannot be made successfully.
3. Driver and its related parts (IC271)
   Constant and IC defects (When it was passed during the adjustment below without going into an abnormal condition)
4. Servo IC (IC201)
   When automatic adjustment was unsuccessful due to defective ICs.

(6) Spindle CLV error

1. When the spindle servo is not locked successfully, RF eye-pattern cannot be locked successfully.
2. IC101"35" (RF OUT), IC101"30" (RF-), IC101"31"(RF+)
3. Is the driver spindle signal input not clipped by the output signal?
4. Is the transistor ON?
5. Defective spindle motor or driver.
6. Other errors may be caused by defective mechanism (jitter) etc. in IC 101 and IC201.

(7) Address Read Failure

The failure may be caused by many possible factors and it is difficult to pick one out. However, the following are among the possible causes.

1. Defective mechanism (significant jitter)
2. IC (IC201, IC301, IC401)
3. Contaminated or damaged discs.

(8) Inter-layer Jump error

1. Defective mechanism.
2. Defective constant or IC of the Driver IC (IC271).
3. Defective servo IC (IC201).

[During Normal Playback of DVD]

(9) No image or sound

1. Search is not possible.
   a) Can the transistor be switched ON?
      If not, see "(5) Tracking ON Error" in "Checkpoints for Individual Errors".
   b) Is the feed operation normal?
      In case of an error, check "(3) Traverse Movement Error" in "Checkpoints for Individual Errors" or check if there is any point where the feed mechanism is caught.

(10) Picture disturbance or unusual sound once every few seconds.

Check if the feed operation during playback is smooth.
↓
If not, perhaps the mechanism is caught.

(11) Others (Example of special cases that occurred in the past)

1. Occasionally, the picture becomes a block or stops.
2. The condition along the innermost perimeter is OK.
   However, at the outermost corner, the picture becomes a block or stops frequently.
   Inaccurate tilting may also be the cause.
   So, perform readjustment of mechanism tilting.

With these symptoms, it is probably a bad jitter value that is causing the problem.

[During normal CD playback]

(12) Is TOC read possible?

NO → Refer to the Servo flow.

CD-DA shows the total time.
V-CD changes to double-speed.
↓ YES
Can it play? NO →

1. The OSD screen shows "NO READING" message.
   (9) As in the case of "Search is not possible", check the feed and tracking.
2. Time display is available, but there is no sound.
   Check DAC, etc. except the Servo.
3. Time flow unstable. Picture abnormal (V-CD).
   Measure the jitter.
4. Check whether the discs is contaminated or damaged.

Precautions for service

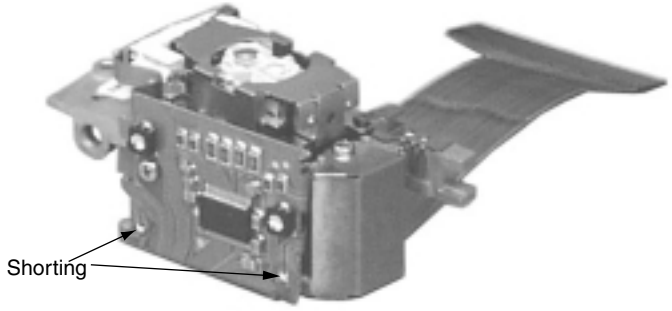
Handling of Traverse Unit and Laser Pickup

1. Do not touch any peripheral element of the pickup or the actuator.
2. The traverse unit and the pickup are precision devices and therefore must not be subjected to strong shock.
3. Do not use a tester to examine the laser diode. (The diode can easily be destroyed by the internal power supply of the tester.)
4. To replace the traverse unit, pull out the metal short pin for protection from charging.
5. When replacing the pickup, after mounting a new pickup, remove the solder on the short land which is provided at the center of the flexible wire to open the circuit.
6. Half-fixed resistors for laser power adjustment are adjusted in pairs at shipment to match the characteristics of the optical block.
   Do not change the setting of these half-fixed resistors for laser power adjustment.

Destruction of Traverse Unit and Laser Pickup by Static Electricity

Laser diodes are easily destroyed by static electricity charged on clothing or the human body. Before repairing peripheral elements of the traverse unit or pickup, be sure to take the following electrostatic protection:

1. Wear an antistatic wrist wrap.
2. With a conductive sheet or a steel plate on the workbench on which the traverse unit or the pick up is to be repaired, ground the sheet or the plate.
3. After removing the flexible wire from the connector (CN101), short-circuit the flexible wire by the metal clip.
4. Short-circuit the laser diode by soldering the land which is provided at the center of the flexible wire for the pickup.
   After completing the repair, remove the solder to open the circuit.

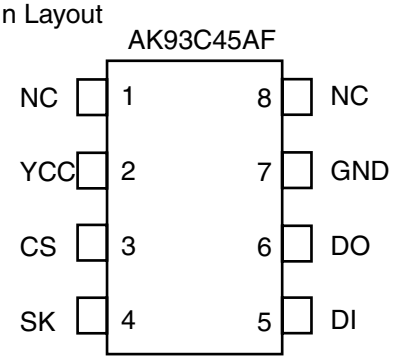


When replacing the Mechanism Unit, turn ON the laser switch that is located at the lower of the pick up after replacement.

Description of major ICs

■ AK93C45AF-W (IC791) : CMOS EEPROM

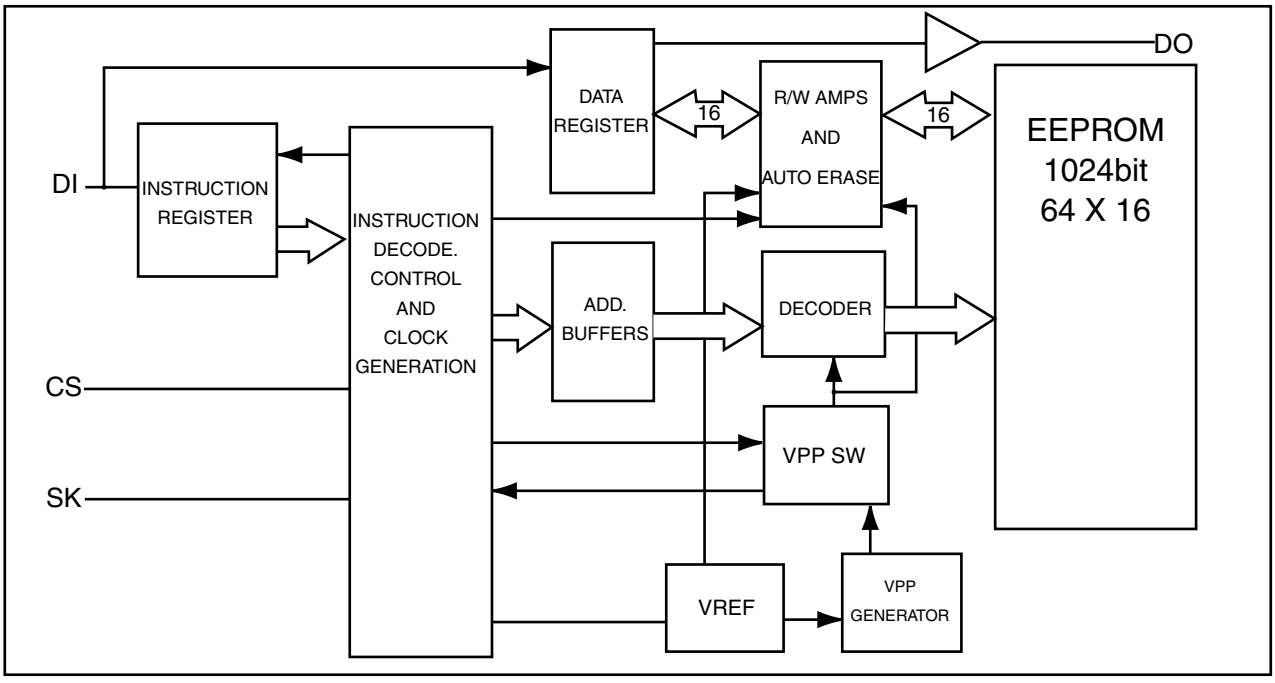
1.Pin Layout



2.Pin Functions

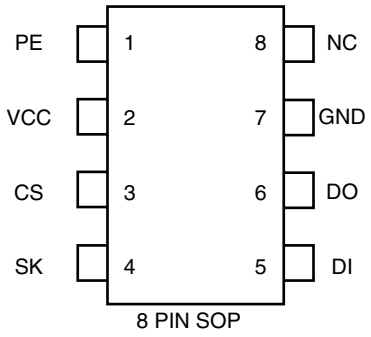
Symbol	Function
CS	Chip Select
SK	Serial Clock Input
DI	Serial Data Input
DO	Serial Data Output
Vcc	Power Supply
GND	Ground
NC	Non connection

3.Block Diagram

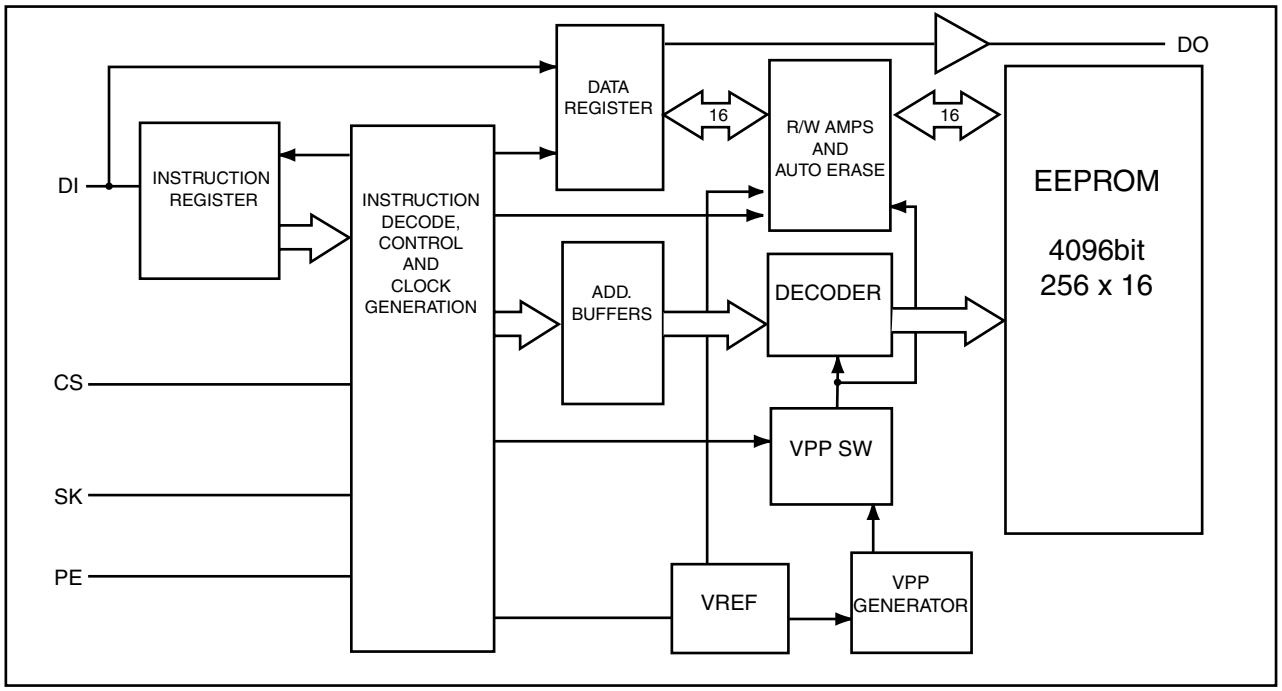


■ AK93C65AF-X (IC403) : EEPROM

1.Terminal layout



2.Block diagram



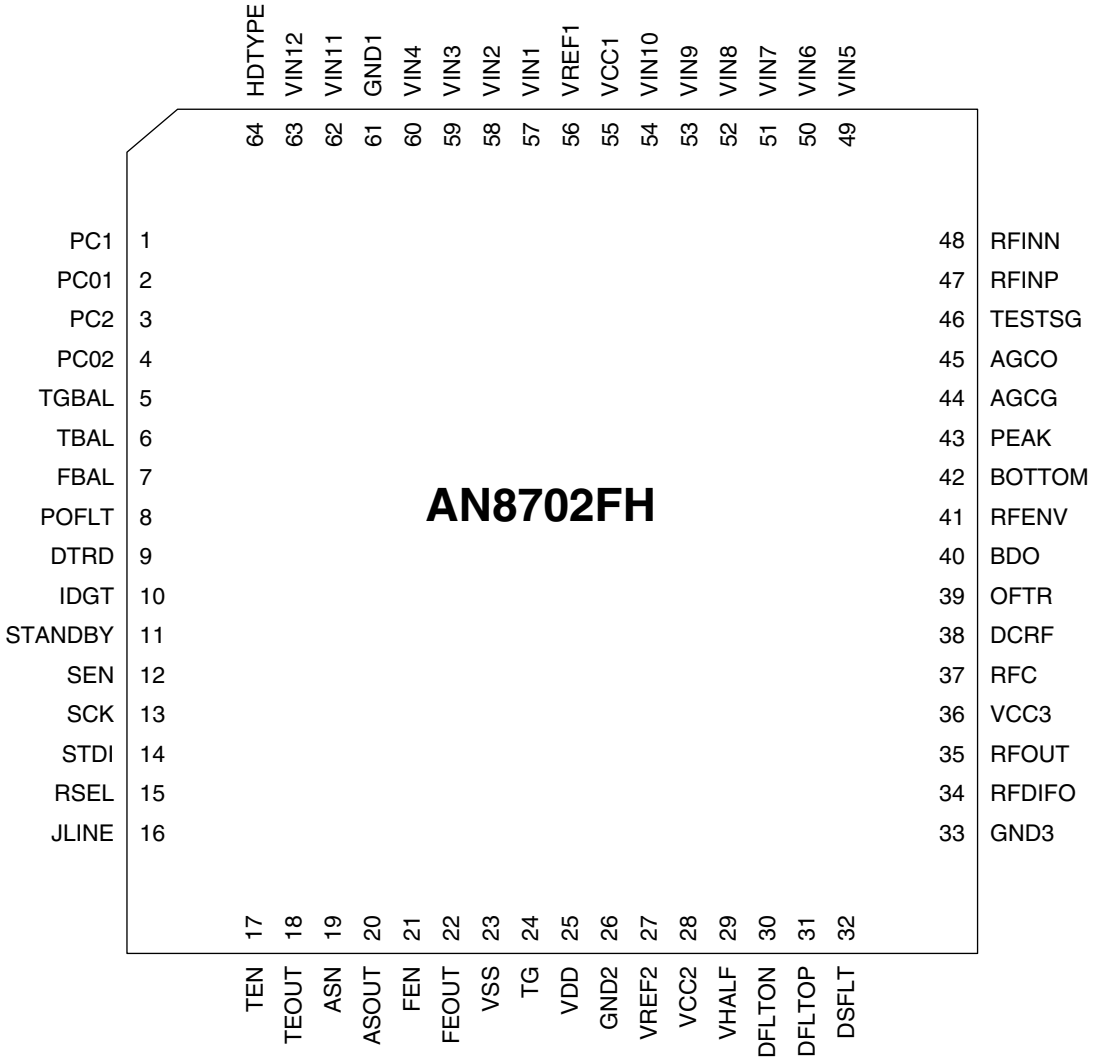
3.Pin function

Pin no.	Symbol	Function
1	PE	Program enable (With built-in pull-up resistor)
2	VCC	Power supply
3	CS	Chip selection
4	SK	Cereal clock input
5	DI	Cereal data input
6	DO	Cereal data output
7	GND	Ground
8	NC	No connection

NOTE : The pull-up resistor of the PE pin is about 2.5M Ω (VCC=5V)

■ AN8702FH (IC101) : Front end processor

1.Terminal Layout



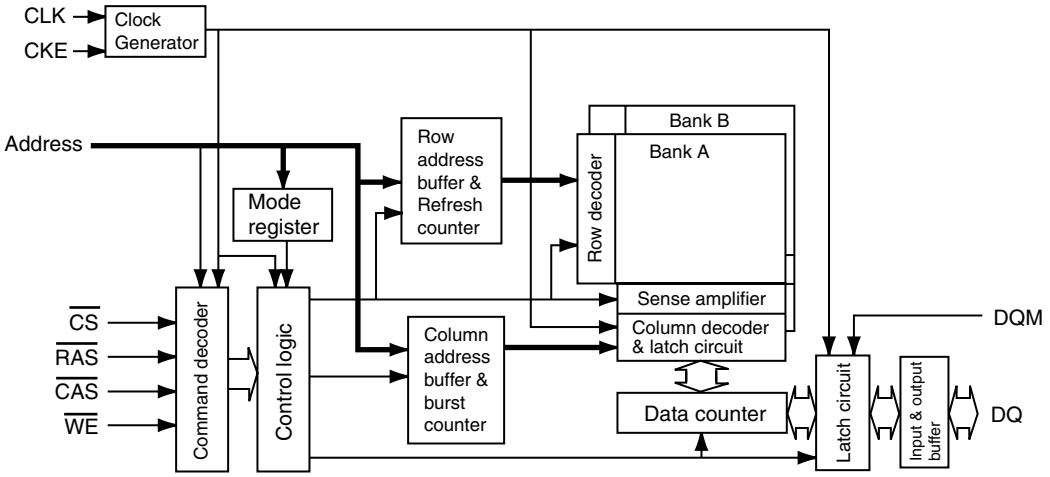
2.Pin Functions

Pin No.	Symbol	I/O	Function
1	PC1		
2	PC01		
3	PC2		
4	PC02		
5	TGBAL	I	Tangential phase balance control terminal
6	TBAL	I	Tracking balance control terminal
7	FBAL	I	Focus balance control terminal
8	POFLT	O	Track detection threshold value level terminal
9	DTRD	I	Data slice part data read signal input terminal (For RAM)
10	IDGT	I	Data slice part address part gate signal input terminal (For RAM)
11	STANDBY	I	Standby mode control terminal
12	SEN	I	SEN (Serial data input terminal)
13	SCK	I	SCK (Serial data input terminal)
14	STDI	I	STDI (Serial data input terminal)
15	RSEL		
16	JLINE		
17	TEN		
18	TEOUT	O	Tracking error signal output terminal

Pin No.	Symbol	I/O	Function
19	ASN		
20	ASOUT		
21	FEN	I	Focus error output amplifier reversing input terminal
22	FEOUT	O	Focus error signal output terminal
23	VSS	-	Ground
24	TG	O	Tangential phase error signal output terminal
25	VDD	-	Apply 3V
26	GND2	-	Ground
27	VREF2	O	VREF2 voltage output terminal
28	VCC2	-	Apply 5V
29	VHALF	O	VHALF voltage output terminal
30	DFLTON		
31	DFLTOP		
32	DSFLT		
33	GND3	-	Ground
34	RFDIFO		
35	RFOUT		
36	VCC3	-	Apply 5V
37	RFC		
38	DCRF	O	All addition amplifier capacitor terminal
39	OFTR	O	OFTR output terminal
40	BDO		
41	RFENV	O	RF envelope output terminal
42	BOTTOM	O	Bottom envelope detection filter terminal
43	PEAK	O	Peak envelope detection filter terminal
44	AGCG	O	AGC amplifier gain control terminal
45	AGCO		
46	TESTSG	I	TEST signal input terminal
47	RFINP	I	RF signal positive input terminal
48	RFINN	I	RF signal negative input terminal
49	VIN5	I	Focus input of external division into two terminal
50	VIN6	I	Focus input of external division into two terminal
51	VIN7	I	
52	VIN8	I	I
53	VIN9	I	
54	VIN10	I	
55	VCC1	-	Apply 5V
56	VREF1	O	VREF1 voltage output terminal
57	VIN1	I	External division into four (DVD/CD) RF input terminal1
58	VIN2	I	External division into four (DVD/CD) RF input terminal2
59	VIN3	I	External division into four (DVD/CD) RF input terminal3
60	VIN4	I	External division into four (DVD/CD) RF input terminal4
61	GND1	-	Ground
62	VIN11	I	
63	VIN12	I	
64	HDTYPE		

■ HY57V161610DTC8 or KM416S1120DT-G8 (IC504,IC505) : 16MB SDRAM

1.Block diagram

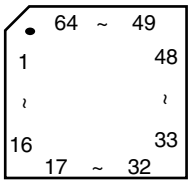


2.Pin function

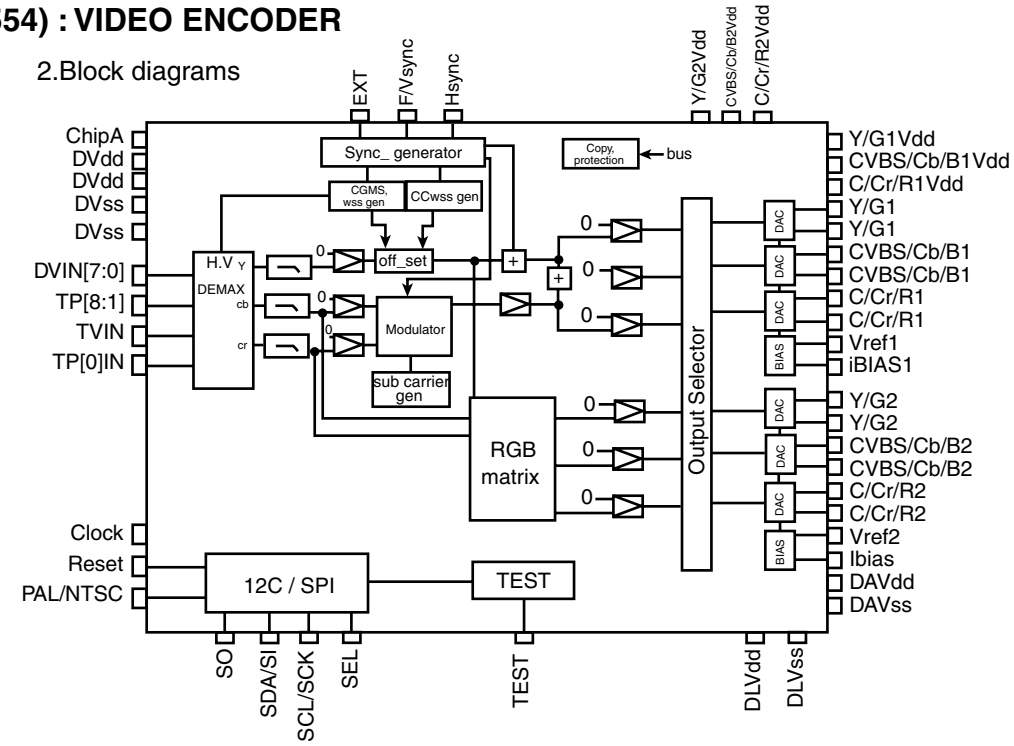
Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	VCC	Power supply	26	VSS	Connect to GND
2,3	DQ0,1	Data input/output	27~32	A4~9	Address inputs
4	VSS	Connect to GND	33	NC	Non connect
5,6	DQ2,3	Data input/output	34	CKE	Clock enable
7	VDD	Power supply	35	CLK	System clock input
8,9	DQ4,5	Data input/output	36	UDQM	Upper DQ mask enable
10	VSS	Connect to GND	37	NC	Non connect
11,12	DQ6,7	Data input/output	38	VCC	Power supply
13	VCC	Power supply	39,40	DQ8,9	Data input/output
14	LDQM	Lower DQ mask enable	41	VSS	Connect to GND
15	$\overline{WE}$	Write enable	42,43	DQ10,11	Data input/output
16	$\overline{CAS}$	Column address strobe	44	VDD	Power supply
17	$\overline{RAS}$	Row address strobe	45,46	DQ12,13	Data input/output
18	$\overline{CS}$	Chip enable	47	VSS	Connect to GND
19,20	A11,10	Address inputs	48,49	DQ14,15	Data input/output
21~24	A0~3	Address inputs	50	VSS	Connect to GND
25	VCC	Power supply			

■ MC44724AVFU (IC554) : VIDEO ENCODER

1.Terminal layout



2.Block diagrams

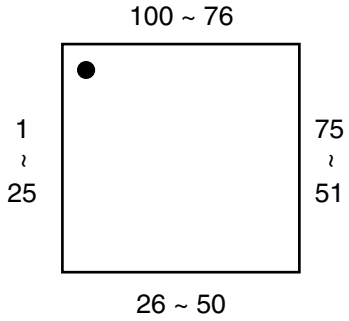


3.Pin function

No.	Symbol	I/O	Function	No.	Symbol	I/O	Function
1	CVBS/Cb/B1	O	Analog composite drive signal (+)	33	SO	-	Non connect
2	$\overline{\text{CVBS/Cb/B1}}$	O	Analog composite drive signal (-)	34	SDA/SI	I	SPI Mode : Serial data input
3	CVBS/Cb/B1Vdd	-	Power supply for CVBS/Cb/B DAC1	35	SCL/SCK	I	Serial clock input
4	Y/G1	O	Analog brightness signal/G drive signal (+)	36	SEL	I	Power supply for serial data,chip select,digital
5	$\overline{\text{Y/G1}}$	O	Analog brightness signal/G drive signal (-)	37	DVdd	--	Power supply for digital circuit
6	Y/G1/Vdd	-	Power supply for Y/G DAC	38	DVss	--	Digital ground
7	C/Cr/R1	O	Analog chroma signal (+)	39	DVIN7	I/O	Y data input / test data I/O
8	$\overline{\text{C/Cr/R1}}$	O	Analog chroma signal (-)	40	DVIN6	I/O	Y data input / test data I/O
9	C/Cr/R1Vdd	-	Power supply for C/Cr/RDAC	41	DVIN5	I/O	Y data input / test data I/O
10	DAVss	-	Connect to ground for DAC	42	DVIN4	I/O	Y data input / test data I/O
11	TBIAS1	O	Standard BIAS for DAC1	43	DVIN3	I/O	Y data input / test data I/O
12	Vref1	-	Standard voltage for DAC1	44	DVIN2	I/O	Y data input / test data I/O
13	DAVdd	-	Power supply for DAC	45	DVIN1	I/O	Y data input / test data I/O
14	Vref2	-	Standard voltage for DAC2	46	DVIN0	I/O	Y data input / test data I/O
15	TBIAS2	O	Standard BIAS for DAC2	47	TVIN	I	VIDEO mute on Reset(0:nomal, 1:mute)
16	NC	-	Non connect	48	EXT	I/O	Frame output / VBI information input
17	CVBS/Cb/B2	O	Analog composite drive signal (+)	49	F/Vsyac	I/O	Frame / Vertical, synchronous I/O
18	CVBS/Cb/B2	O	Analog composite drive signal (-)	50	Chsyac	I/O	The horizontal, synchronous I/O
19	CVBS/Cb/B2Vdd	-	Power supply for CVBS/Cb/B DAC2	51	DATST	I	Data input
20	Y/G2	O	Analog brightness signal/G drive signal (+)	52	TP-8	I/O	Multiplex data input
21	$\overline{\text{Y/G2}}$	O	Analog brightness signal/G drive signal (-)	53	TP7	I/O	Multiplex data input
22	Y/GVdd	-	Power supply for Y/G DAC	54	TP6	I/O	Multiplex data input
23	C/Cr/R2	O	Analog chroma signal (+)	55	TP5	I/O	Multiplex data input
24	$\overline{\text{C/Cr/R2}}$	O	Analog chroma signal (-)	56	DVss	-	Ground for digital circuit
25	C/Cr/R2Vdd	-	Power supply for C/Cr/RDAC2	57	DVdd	-	Power supply for digital circuit
26	ChipA	-	Chip address selection	58	TP4	I/O	Data input / Test data I/O
27	TEST	I	Connect to test pin	59	TP3	I/O	Data input / Test data I/O
28	DVdd	-	Digital ground	60	TP2	I/O	Data input / Test data I/O
29	CLOCK	I	Clock signal input (27MHz)	61	TP1	I/O	Data input / Test data I/O
30	DVss	-	Power supply for digital circuit	62	TP0	I/O	Data input / Test data I/O
31	Reset	I	Reset signal input L:ON	63	DLVdd	-	Power supply for D/A converter
32	PAL/NTSC	I	Selection NTSC/PAL NTSC:L PAL:H	64	DLVss	-	Ground for D/A converter

■ MN101C12GHA (IC701) : System micom

1.Terminal layout



2.Pin function

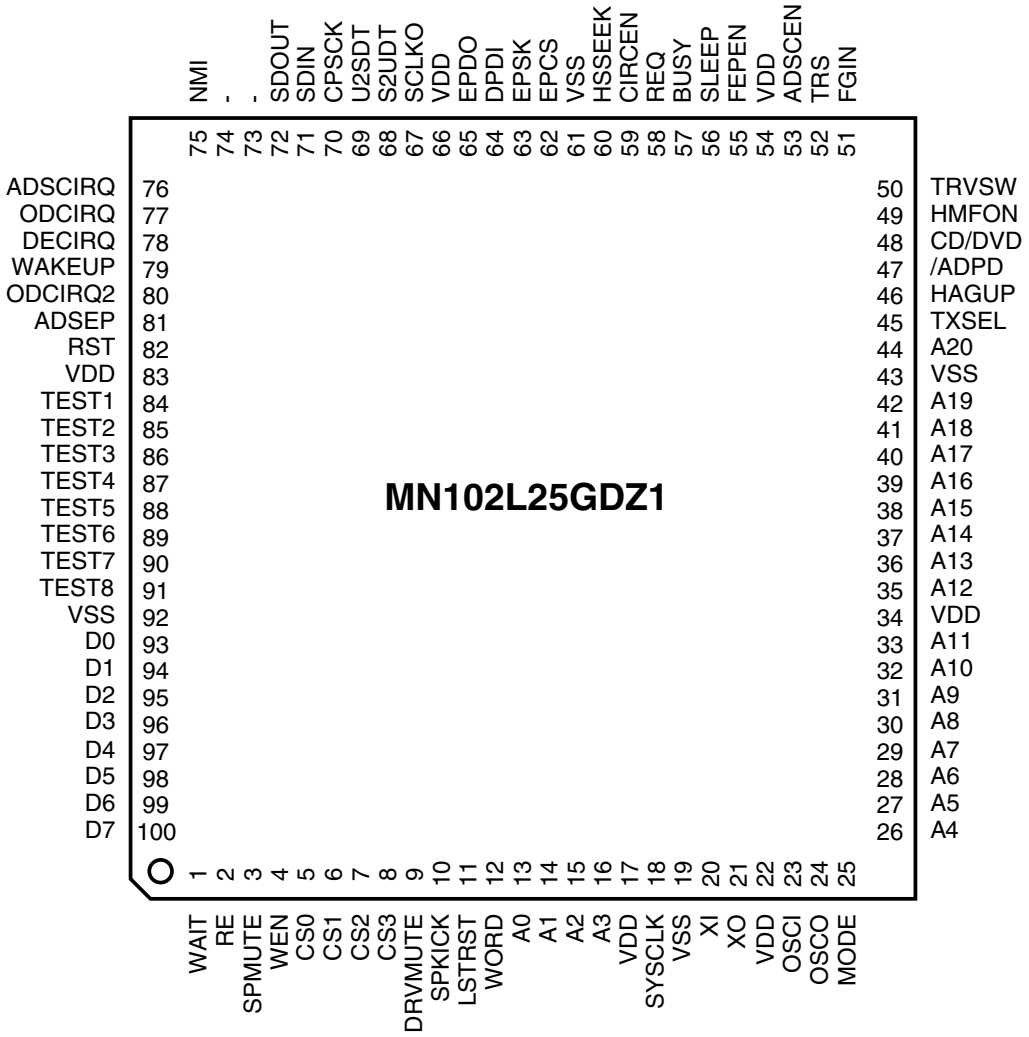
Pin No.	Symbol	I/O	Function
1	GND	-	
2	CS0	I	Setup bit 0 (Effective with U/E versions) software pull-up? available.
3	CS1	I	Setup bit 1 (Effective with U/E versions) software pull-up? available.
4	CS2	I	Setup bit 2 (Effective with U/E versions) software pull-up? available.
5	NTSEL	I	NTSC/PAL Input select switch
6	POWERSW	I	Power key Input
7	SAFETEY	I	
8		I	
9		I	
10	VREF+	-	
11	VDD	-	
12	OSC2	O	10MHz
13	OSC1	I	
14	VSS	-	
15	-	I	Not used. Connect to GND
16	-	O	Not used.
17	MMOD	I	Connect to GND
18	OSDCS3	O	V. ENCODER Chip select
19	RSTE	O	V. ENCODER Reset
20	OSDDO	O	V.ENCODER Communications DATA
21	S2UDT	O	Communications DATA OUT between the Unit and the Microprocessor
22	U2SDT	I	Communications DATA IN between the Unit and the Microprocessor
23	SCLK	O	Communications CLK between the Unit and the Microprocessor
24	BUSY	O	Communications BUSY between the Unit and the Microprocessor
25	CPURST	O	Unit microprocessor Reset
26	REQ	I	Communications REQ between the Unit and the Microprocessor
27	REMO	I	Remote control interruption
28	CS3	I	Setup password change judging bit (H change, L Normally)
29		I	
30	TEST	I	H: Checker mode, L: Normal mode
31	TEST	I	
32		I	
33	RESET	I	Reset Input
34	MT0	O	Tray motor control 0
35	MT1	O	Tray motor control 1
36		O	
37	OSDCK	O	V. ENCODER Communications CK
38	NT	O	NTSC/PAL Switching (V. ENCODER)
39	FS2	O	48kHz/96kHz Switching
40	OPEN	I	Tray OPEN Switch detection Software pull-up??? available
41	CLOSE	I	Tray CLOSE Switch detection Software pull-up??? available
42		O	
43		O	
44		O	
45	FLDATAO	O	FL Driver Communications DATA 0

MN101C12GHA (2/2)

Pin No.	Symbol	I/O	Function
46	FLDATAI	I	FL Driver Communications DATA 1
47	FLCK	O	FL Driver Communications CLOCK
48	FLCS	O	FL Driver Communications CS
49	FLRST	O	
50	EEDO	O	EEPROM Communications DATA 0
51	EEDI	I	EEPROM Communications DATA 1
52	EECK	O	EEPROM Communications CLOCK
53	EECS	O	EEPROM Communications CS
54	VS1	O	S1 Control
55	VS3	O	S3 Control (STBY:H, P.ON:L)
56		O	
57		O	
58		O	
59		O	
60		O	
61		O	
62		O	
63	KARAOKE	O	KARAOKE Gain Control (For KARAOKE, set H)
64	POWERON	O	POWER ON OUTPUT
65		O	
66		O	
67		O	
68		O	
69		O	
70		O	
71		O	
72		O	
73		O	
74		O	
75		O	
76		O	
77	AVC1	I	AV COMPULINK INPUT
78	AVCO	O	AV COMPULINK OUTPUT
79		O	
80	STANBYIND	O	STANDBY LED OUTPUT
81		O	
82		O	
83		O	
84		O	
85		O	
86		O	
87	MA	O	DAC Control MA
88	MB	O	DAC Control MB
89	M1M3	O	DAC Control M1M3
90	MD	O	DAC Control MD
91	MC	O	DAC Control MC
92		O	
93		O	
94		O	
95	DAVSS	-	
96		O	
97		O	
98		O	
99	MUTE	O	Front Mute OUTPUT
100	DAVDD	-	

■ MN102L25GDZ1 (IC401) : UNIT CPU

1.Terminal layout

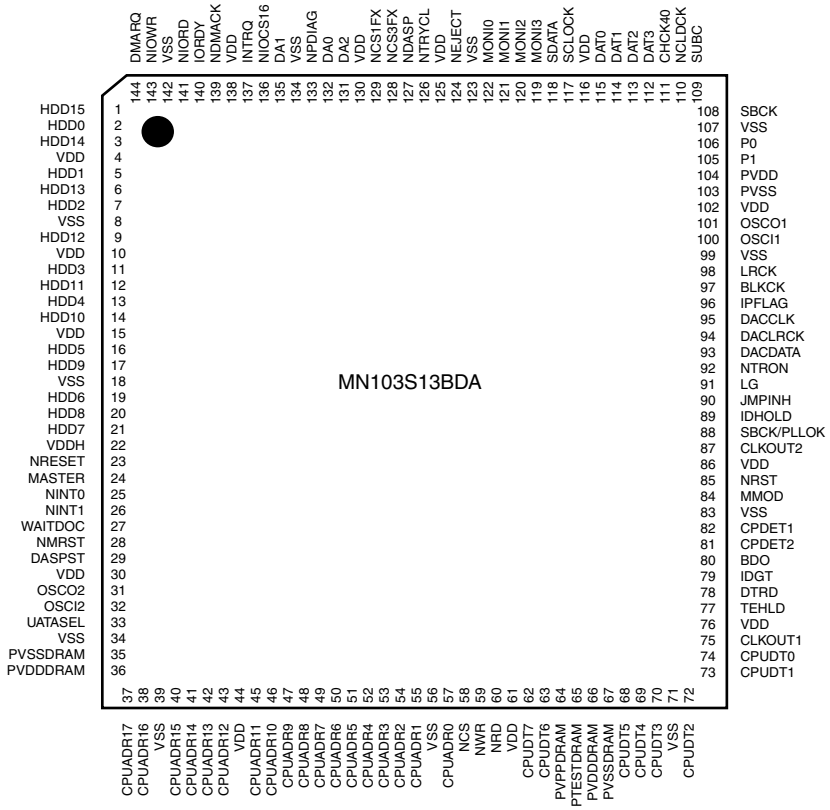


2.Pin function

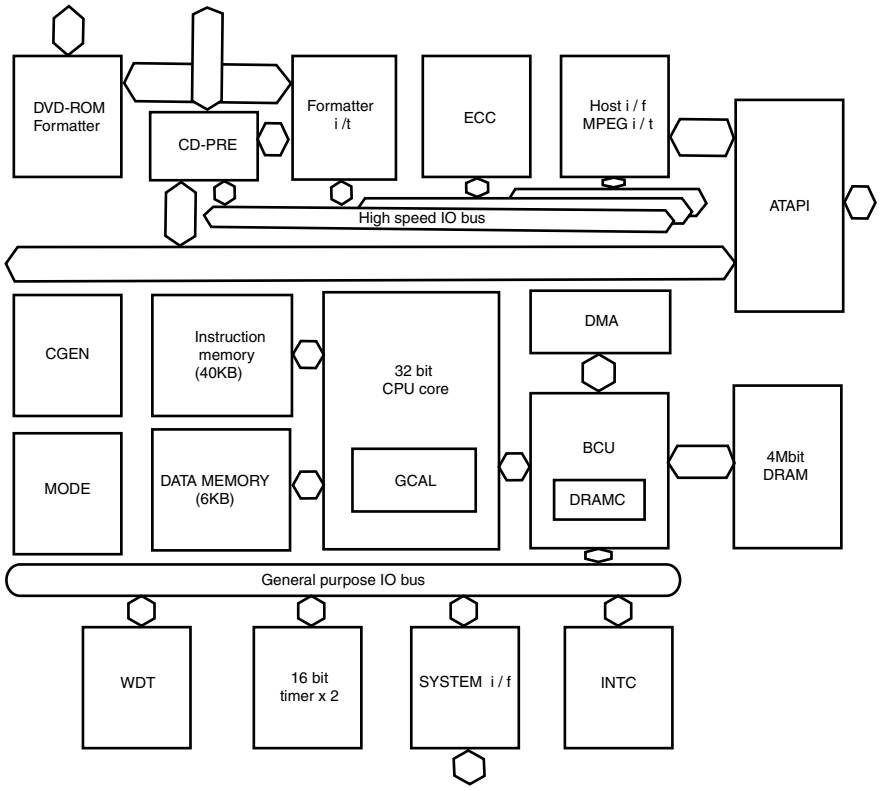
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	WAIT	I	Micon wait signal input	51	FGIN	I	Photo input
2	RE	O	Read enable	52	TRS		
3	SPMUTE	O		53	ADSCEN	O	Serial enable signal for ADSC
4	WEN	O	Write enable	54	VDD	-	Power supply
5	CS0	O	Non connect	55	FEPEN	O	Serial enable signal for FEP
6	CS1	O	Chip select for ODC	56	SLEEP	O	Standby signal for FEP
7	CS2	O	Chip select for ZIVA	57	BUSY	I	Communication busy
8	CS3	O	Chip select for outer ROM	58	REQ	O	Communication Request
9	DRVMUTE	O	Driver mute	59	CIRCEN	O	CIRC command select
10	SPKICK	O	Spin kick (Non connect)	60	HSSEEK	O	Seek select
11	LSIRST	O	LSI reset	61	VSS	-	Ground
12	WORD	O	Bus selection input	62	EPCS	O	EEPROM chip select
13	A0	O	Address bus 0 for CPU	63	EPSK	O	EEPROM clock
14	A1	O	Address bus 1 for CPU	64	DPDI	I	EEPROM data input
15	A2	O	Address bus 2 for CPU	65	EPDO	O	EEPROM data output
16	A3	O	Address bus 3 for CPU	66	VDD	-	Power supply
17	VDD	-	Power supply	67	SCLKO	I	Communication clock
18	SYSCLK	O	System clock signal output	68	S2UDT	I	Communication input data
19	VSS	-	Ground	69	U2SDT	O	Communication output data
20	XI	-	Not use (Connect to vss)	70	CPSCK	O	Clock for ADSC serial
21	XO	-	Non connect	71	SDIN	I	ADSC serial data input
22	VDD	-	Power supply	72	SDOUT	O	ADSC serial data output
23	OSCI	I	Clock signal input(13.5MHz)	73	-	-	Not use
24	OSCO	O	Clock signal output(13.5MHz)	74	-	-	Not use
25	MODE	I	CPU Mode selection input	75	NMI	-	Not use
26	A4	O	Address bus 4 for CPU	76	ADSCIRQ	I	Interrupt input of ADSC
27	A5	O	Address bus 5 for CPU	77	ODCIRQ	I	Interrupt input of ODC
28	A6	O	Address bus 6 for CPU	78	DECIRQ	I	Interrupt input of ZIVA
29	A7	O	Address bus 7 for CPU	79	WAKEUP	O	Not use
30	A8	O	Address bus 8 for CPU	80	ODCIRQ2	I	
31	A9	O	Address bus 9 for CPU	81	ADSEP	I	Address data selection input
32	A10	O	Address bus 10 for CPU	82	RST	I	Reset input
33	A11	O	Address bus 11 for CPU	83	VDD	-	Power supply
34	VDD	-	Power supply	84	TEST1	I	Test signal 1 input
35	A12	O	Address bus 12 for CPU	85	TEST2	I	Test signal 2 input
36	A13	O	Address bus 13 for CPU	86	TEST3	I	Test signal 3 input
37	A14	O	Address bus 14 for CPU	87	TEST4	I	Test signal 4 input
38	A15	O	Address bus 15 for CPU	88	TEST5	I	Test signal 5 input
39	A16	O	Address bus 16 for CPU	89	TEST6	I	Test signal 6 input
40	A17	O	Address bus 17 for CPU	90	TEST7	I	Test signal 7 input
41	A18	O	Address bus 18 for CPU	91	TEST8	I	Test signal 8 input
42	A19	O	Address bus 19 for CPU	92	VSS	-	Ground
43	VSS	-	Ground	93	D0	I/O	Data bus 0 of CPU
44	A20	O	Address bus 20 for CPU	94	D1	I/O	Data bus 1 of CPU
45	TXSEL	O	TX Select	95	D2	I/O	Data bus 2 of CPU
46	HAGUP	O		96	D3	I/O	Data bus 3 of CPU
47	/ADPD			97	D4	I/O	Data bus 4 of CPU
48	CD/DVD	O		98	D5	I/O	Data bus 5 of CPU
49	HMFON			99	D6	I/O	Data bus 6 of CPU
50	TRVSW	I	Detection switch of traverse inside	100	D7	I/O	Data bus 7 of CPU

MN103S13BDA (IC301) : Optical disc controller

1.Terminal layout



2.Block diagram



3.Pin function

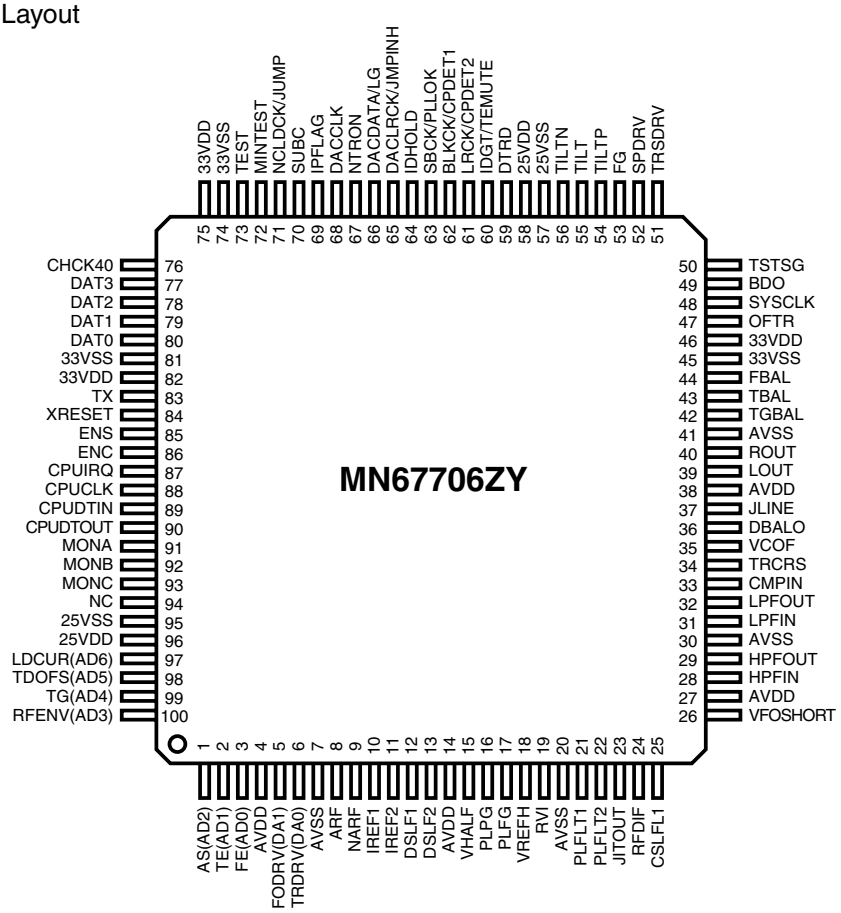
Pin NO.	Symbol	I/O	Function
1	HDD15	I/O	ATAPI data
2	HDD0	I/O	ATAPI data
3	HDD14	I/O	ATAPI data
4	VDD	-	Apply 3V
5	HDD1	I/O	ATAPI data
6	HDD13	I/O	ATAPI data
7	HDD2	I/O	ATAPI data
8	VSS	-	GND
9	HDD12	I/O	ATAPI data
10	VDD	-	Apply 2.7V
11	HDD3	I/O	ATAPI data
12	HDD11	I/O	ATAPI data
13	HDD4	I/O	ATAPI data
14	HDD10	I/O	ATAPI data
15	VDD	-	Apply 3V
16	HDD5	I/O	ATAPI data
17	HDD9	I/O	ATAPI data
18	VSS	-	GND
19	HDD6	I/O	ATAPI data
20	HDD8	I/O	ATAPI data
21	HDD7	I/O	ATAPI data
22	VDDH		
23	NRESET	I	ATAPI reset
24	MASTER	I/O	ATAPI master / slave selection
25	NINT0	O	System control interruption 0
26	NINT1	O	System control interruption 1
27	WAITDOC	O	System control wait control
28	NMRST	O	System control reset (Connect to TP302)
29	DASPST	I	DASP signal initializing (VSS connected)
30	VDD	-	Apply 3V
31	OSCO2	O	OPEN (Connect to TP140)
32	OSCI2	I	OPEN (Connect to TP303)
33	UATASEL	I	VSS connected
34	VSS	-	GND
35	PVSSDRAM		VSS connected
36	PVDDDRAM		VDD (2.7V) connected
37	CPUADR17	I	System control address
38	CPUADR16	I	System control address
39	VSS	-	GND
40	CPUADR15	I	System control address
41	CPUADR14	I	System control address
42	CPUADR13	I	System control address
43	CPUADR12	I	System control address
44	VDD	-	Apply 2.7V
45	CPUADR11	I	System control address
46	CPUADR10	I	System control address
47	CPUADR9	I	System control address
48	CPUADR8	I	System control address
49	CPUADR7	I	System control address
50	CPUADR6	I	System control address

Pin NO.	Symbol	I/O	Function
51	CPUADR5	I	System control address
52	CPUADR4	I	System control address
53	CPUADR3	I	System control address
54	CPUADR2	I	System control address
55	CPUADR1	I	System control address
56	VSS	-	GND
57	CPUADR0	I	System control address
58	NCS	I	System control chip selec
59	NWR	I	System control write
60	NRD	I	System control read
61	VDD	-	Apply 3V
62	CPUDT7	I/O	System control data
63	CPUDT6	I/O	System control data
64	PVPPDRAM	O	VSS connected
65	PTESTDRAM	I	VSS connected
66	PVDDDRAM		VDD (2.7V) connected
67	PVSSDRAM		VSS connected
68	CPUDT5	I/O	System control data
69	CPUDT4	I/O	System control data
70	CPUDT3	I/O	System control data
71	VSS	-	GND
72	CPUDT2	I/O	System control data
73	CPUDT1	I/O	System control data
74	CPUDT0	I/O	System control data
75	CLKOUT1	O	16.9/11.2/8.45MHz clock
76	VDD	-	Apply 3V
77	TEHLD	O	Mirror gate (Connect to TP141)
78	DTRD	O	Data part frequency control switch (Connect to TP304)
79	IDGT	O	Part CAPA switch (Connect to TP305)
80	BDO	I	RF dropout / BCA data of making to binary
81	CPDET2	I	Outer side CAPA detection
82	CPDET1	I	Side of surroundings on inside
83	VSS	-	GND
84	MMOD	I	VSS connected
85	NRST	I	System reset
86	VDD	-	Apply 3V
87	CLKOUT2	O	16.9MHz clock
88	SBCK/PLLOK	O	Frame mark detection
89	IDOHOLD	O	ID gate for tracking holding (Connect to TP307)
90	JMPINH	O	Jump prohibition
91	LG	O	Land / group switch
92	NTRON	I	Tracking ON
93	DACDATA	O	Sereal output (Connect to TP148)
94	DACLRCK	O	L and R identification output (Connect to TP149)
95	DACCLK	I	Clock for serial output
96	IPFLAG	I	Interpolation flag input
97	BLKCK	I	Sub-code,Block clock input (VSS connected)
98	LRCK	I	L and R identification signal output (VSS connected)
99	VSS	-	GND
100	OSCI1	I	16.9MHz oscillation

Pin NO.	Symbol	I/O	Function
101	OSCO1	O	16.9MHz oscillation
102	VDD	-	Apply 3V
103	PVSS	-	GND
104	PVDD	-	Apply 3V
105	P1	I/O	Terminal MASTER polarity switch input (VDD 3V connected)
106	P0	I/O	CIRC-RAM OVER/UNDER Interruption signal input (VDD 3V connected)
107	VSS	-	GND
108	SBCK	O	Sub-code, Clock output for serial input (Connect to TP306)
109	SUBC	I	Sub-code, Serial input
110	NCLDCK	I	Sub-code, Frame clock input
111	CHCK40	I	Read clock to DAT3~0 (Output of dividing frequency four from ADSC)
112	DAT3	I	Read data from DISC (Parallel output from ADSC)
113	DAT2	I	
114	DAT1	I	
115	DAT0		
116	VDD	-	Apply 3V
117	SCLOCK	I/O	Debugging serial clock (Not use) (270Ωpull up)
118	SDATA	I/O	Debugging serial data (Not use) (270Ωpull up)
119	MONI3	O	Internal goods title monitor (Connect to TP150-TP153)
120	MONI2	O	
121	MONI1	O	
122	MONI0	O	
123	VSS	-	GND
124	NEJECT	I	Eject detection
125	VDD	-	Apply 2.7V
126	NTRYCL	I	Tray close detection (Not use)
127	NDASP	I/O	ATAPI Drive active/ Slave connection I/O
128	NCS3FX	I	ATAPI host chip selec (Not use)
129	NCS1FX	I	ATAPI host chip selec (Not use)
130	VDD	-	Apply 3V
131	DA2	I/O	ATAPI host address
132	DA0	I/O	ATAPI host address (Not use)
133	NPDIAG	I/O	ATAPI slave master diagnosis input
134	VSS	-	GND
135	DA1	I/O	ATAPI host address (Not use)
136	NIOCS16	O	ATAPI output of selection of width of host data bus
137	INTRQ	O	ATAPI host interruption output
138	VDD	-	Apply 3V
139	NDMACK	I	ATAPI host DMA response (Not use)
140	IORDY	O	ATAPI host ready output (Connect to TP157)
141	NIORD	I	ATAPI host read (Not use)
142	VSS	-	GND
143	NIOWR	I/O	ATAPI host writes
144	DMARQ	O	ATAPI host DMA request (Connect to TP159)

■ MN67706ZY (IC201) : ADSC

1.Terminal Layout



2.Pin Functions

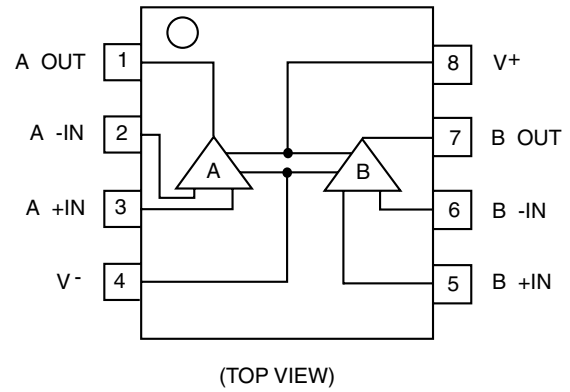
Pin No.	Symbol	I/O	Function
1	AS(AD2)	I	AS : Full adder signal(FEP)
2	TE(AD1)	I	Phase difference/3 beam tracking error(FEP)
3	FE(AD0)	I	Focus error(FEP)
4	AVDD	-	Apply 3.3V(For analog circuit)
5	FODRV(DA1)	O	Focus drive(DRVIC)
6	TRDRV(DA0)	O	Tracking drive(DRVIC)
7	AVSS	-	Ground(For analog circuit)
8	ARF	I	Equivalence RF+(FEP)
9	NARF	I	Equivalence RF-(FEP)
10	IREF1	I	Reference current1(For DBAL)
11	IREF2	I	Reference current2(For DBAL)
12	DSLF1	I/O	Connect to capacitor1 for DSL
13	DSLF2	I/O	Connect to capacitor2 for DSL
14	AVDD	-	Apply 3.3V(For analog circuit)
15	VHALF	I	Reference voltage 1.65+-0.1V(FEP)
16	PLPG	-	Not use(PLL phase gain setting resistor terminal)
17	PLFG	-	Not use(PLL frequency gain setting resistor terminal)
18	VREFH	I	Reference voltage 2.2V+-0.1V(FEP)
19	RVI	I/O	Connect to resistor for VREFH reference current source
20	AVSS	-	Ground(For analog circuit)
21	PLFLT1	O	Connect to capacitor1 for PLL
22	PLFLT2	O	Connect to capacitor2 for PLL
23	JITOUT	I/O	Output for jitter signal monitor
24	RFDIF	I	Not use
25	CSLFL1	I/O	Pull-up to VHALF

Pin No.	Symbol	I/O	Function
26	VFOSHORT	O	VFO short output
27	AVDD	-	Apply 3.3V(For analog circuit)
28	HPFIN	I	Pull-up to VHALF
29	HPFOUT	O	Connect to TP208
30	AVSS	-	Ground(For analog circuit)
31	LPFIN	I	Pull-up to VHALF
32	LPFOUT	O	Not use
33	CMPIN	I	Connect to TP210
34	TRCRS	I	Input signal for track cross formation
35	VCOF	I/O	JFVCO control voltage
36	DBALO	O	DSL balance adjust output
37	JLINE	O	J-line setting output(FEP)
38	AVDD	-	Apply 3.3V(For analog circuit)
39	LOUT	O	Connect to TP203 (Analog audio left output)
40	ROUT	O	Connect to TP204 (Analog audio right output)
41	AVSS	-	Ground(For analog circuit)
42	TGBAL	O	Tangential balance adjust(FEP)
43	TBAL	O	Tracking balance adjust(FEP)
44	FBAL	O	Focus balance adjust(FEP)
45	33VSS	-	Ground(For I/O)
46	33VDD	-	Apply 3.3V(For I/O)
47	OFTR	I	Off track signal
48	SYSCLK	I	16.9344MHz system clock input(ODC)
49	BDO	I	Drop out(FEP)
50	TSTSG	O	Calibration signal(FEP)
51	TRSDRV	O	Traverse drive(DRVIC)
52	SPDRV	O	Spindle drive output(DRVIC)
53	FG	I	FG signal input (Spindle motor driver)
54	TILTP	O	Connect to TP205
55	TILT	O	Connect to TP206
56	TILTN	O	Connect to TP207
57	25VSS	-	Ground(For internal core)
58	25VDD	-	Apply 2.5V(For internal core)
59	DTRD	I	Data read control signal(ODC)
60	IDGT/TEMUTE	I	Pull-down to Ground
61	LRCK/CPDET2	O	LR channel data strobe(ODC)/
62	BLKCK/CPDET1	O	CD sub code synchronous signal(ODC)/
63	SBCK/PLLOK	I	CD sub code data shift clock(ODC)/PLL pull-in OK signal input
64	IDHOLD	I	Pull-down to Ground
65	DACLRCK/JMPINH	I	1bit DAC-LR channel data strobe(ODC)/
66	DACDATA/LG	I	CD 1bit DAC channel data(ODC)
67	NTRON	O	L : Tracking ON(ODC)
68	DACCLK	O	1bit DAC channel data shift clock(ODC)
69	IPFLAG	O	CIRC error flag(ODC)
70	SUBC	O	CD sub code(ODC)
71	NCLDCK/JUMP	O	CD sub code data frame clock(ODC)/DVD JUMP signal(ODC)
72	MINTEST	I	Pull-down to Ground(For MINTEST)
73	TEST	I	Pull-down to Ground(For TEST)
74	33VSS	-	Ground(For I/O)
75	33VDD	-	Apply 3.3V(For I/O)
76	CHCK40	O	Clock for SRDATA(ODC)
77	DAT3	O	SRDATA3(ODC)
78	DAT2	O	SRDATA2(ODC)
79	DAT1	O	SRDATA1(ODC)
80	DAT0	O	SRDATA0(ODC)

Pin No.	Symbol	I/O	Function
81	33VSS	-	Ground(For I/O)
82	33VDD	-	Apply 3.3V(For I/O)
83	TX	O	Digital audio interface
84	XRESET	I	Reset input (System control)
85	ENS	I	Servo DSC serial I/F chip select (System control)
86	ENC	I	CIRC serial I/F chip select (System control)
87	CPUIRQ	O	Interrupt request (System control)
88	CPUCLK	I	Syscon serial I/F clock (System control)
89	CPUDTIN	I	Syscon serial I/F data input (System control)
90	CPUDTOUT	O	Syscon serial I/F data output (System control)
91	MONA	O	Connect to TP226 (Monitor terminal A)
92	MONB	O	Connect to TP225 (Monitor terminal A)
93	MONC	O	Connect to TP224 (Monitor terminal A)
94	NC	O	Connect to TP211
95	25VSS	-	Ground(For internal core)
96	25VDD	-	Apply 2.5V(For internal core)
97	LDCUR(AD6)	I	
98	TDOFS(AD5)	I	
99	TG(AD4)	I	Tangential phase difference(FEP)
100	RFENV(AD3)	I	RF envelope input(FEP)

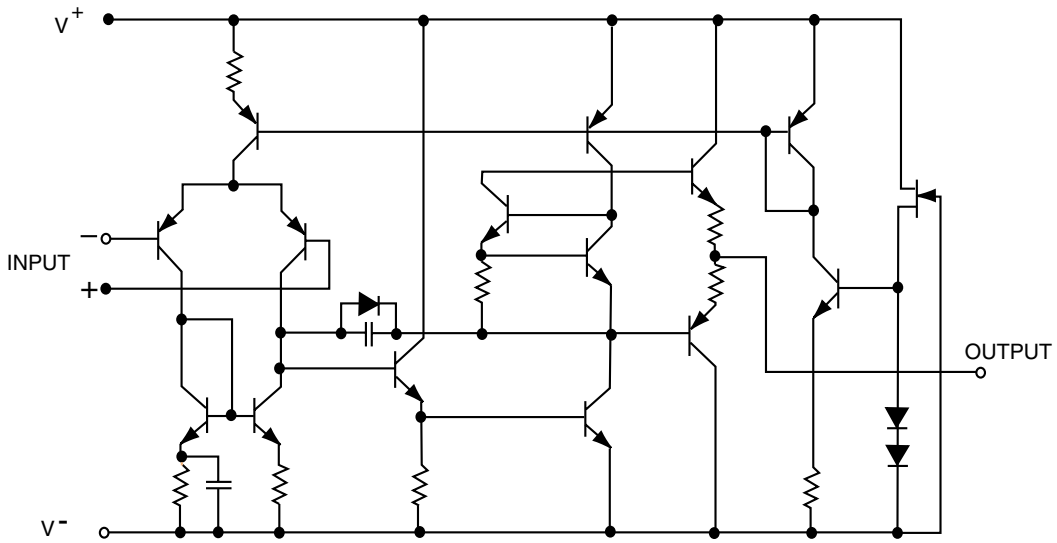
■ NJM4580D (IC741, IC751) : LPF, Mic and H.phone Amp.

1.Terminal layout



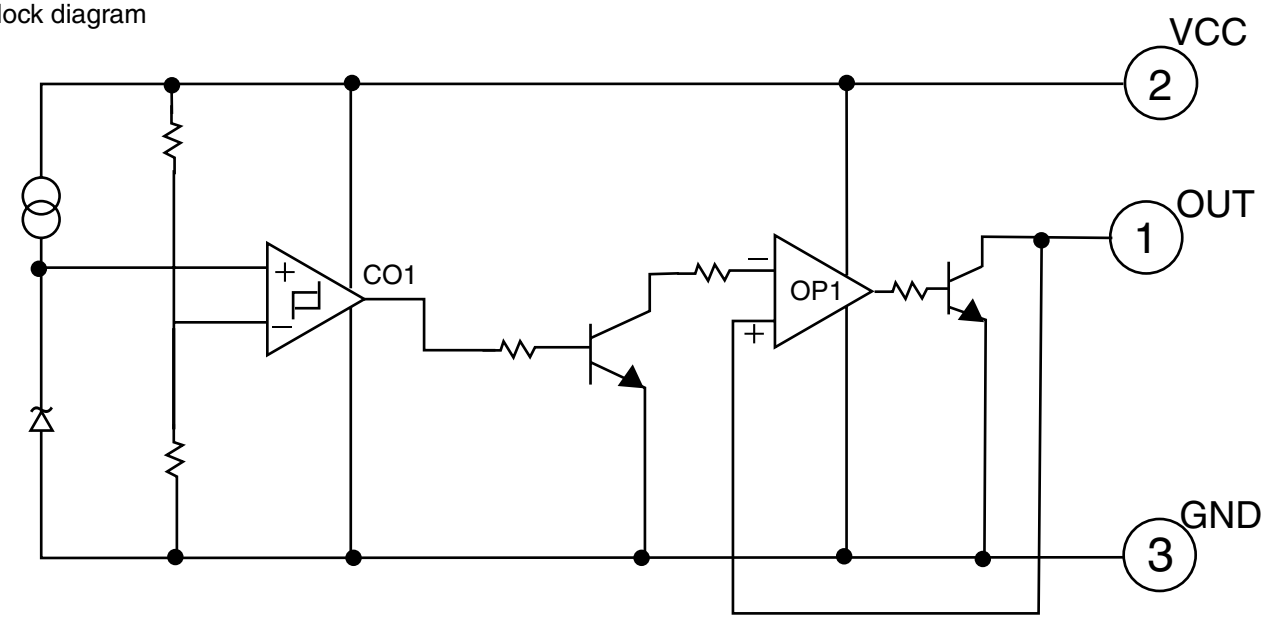
(TOP VIEW)

2.Block diagram



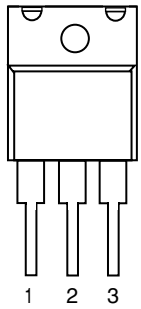
■ IC-PST9140-T (IC702) : Reset IC

1. Block diagram



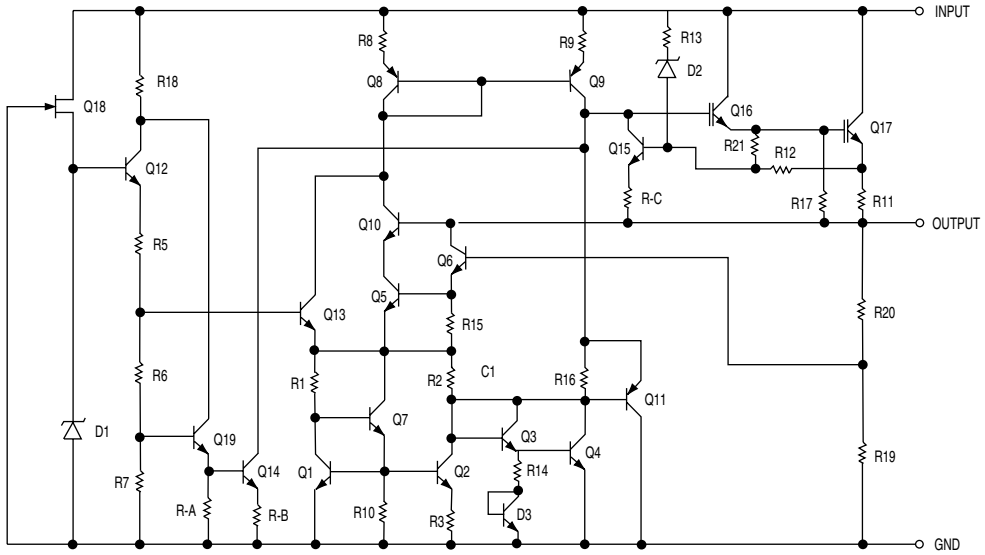
■ NJM78M05FA (IC953) : Regulator

1. Terminal layout

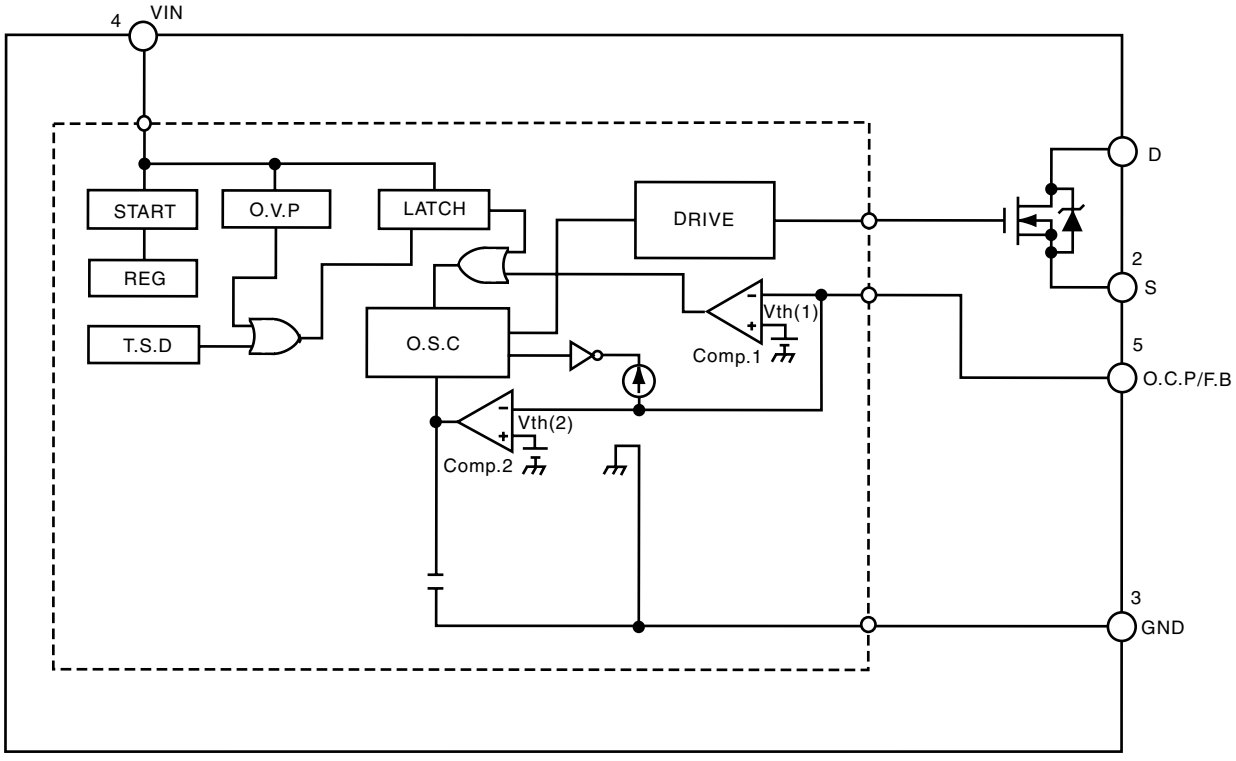


1. INPUT
2. GND
3. OUTPUT

2. Block diagram

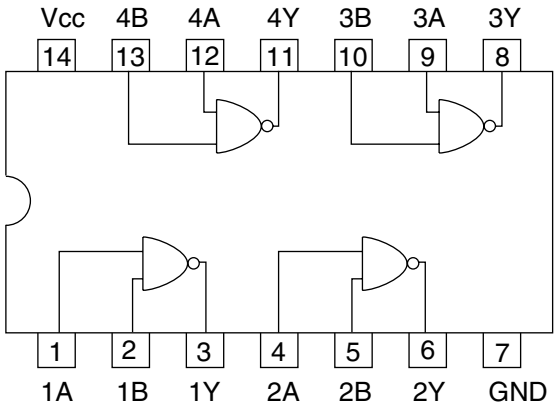


■ STR-G6651 (IC901) : Switch regulator



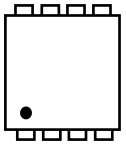
■ TC74VHC00FT-X (IC503) : Wright timing control

1.Terminal layout / Block diagram

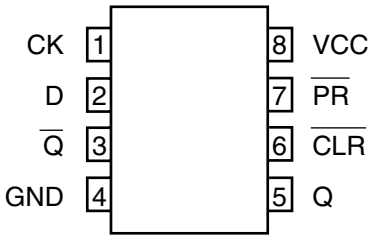


■ TC7WH74FU-X (IC374) : Clock buffer

1.Terminal layout

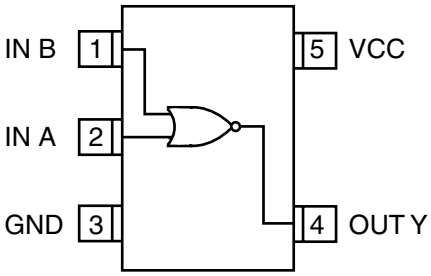


2.Block diagram



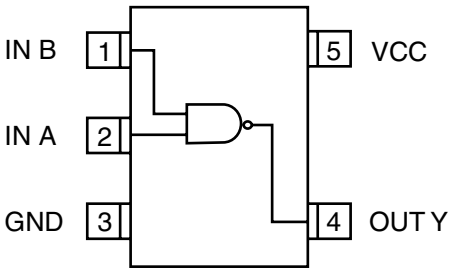
■ TC7SH32FU-X (IC312) : Timing control

1.Terminal layout



■ TC7SH08FU-X (IC311) : Timing control

1.Terminal layout



■ ZIVA3-PE0 (IC501) : AV Decoder

ZIVA3-PEO (1/5)

Pin No.	Symbol	I/O	Function
1	PIO0	I/O	Programmable I/O pins.Input mode after reset.
2	HDATA0	I/O	8-bit bi-derectional host data bus. writes data to the decoder Code FIFO via HDATA. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM via HDATA.
3	HDATA1		
4	HDATA2		
5	VDD-3.3	-	3.3-V supply voltage for I/O signals.
6	HDATA3	I/O	8-bit bi-derectional host data bus. writes data to the decoder Code FIFO via HDATA. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM via HDATA.
7	VSS	-	Ground for core logic and I/O signals.
8	HDATA4	I/O	8-bit bi-derectional host data bus. writes data to the decoder Code FIFO via HDATA. MSB of the 32-bit word is written first. The host also reads and writes the decoder internal registers and local SDRAM via HDATA.
9	HDATA5		
10	HDATA6		
11	HDATA7		
12	VDD-2.5	-	2.5-V supply voltage for core logic.
13	$\overline{\text{RESET}}$	I	Hardware reset. An external device asserts $\overline{\text{RESET}}$(active LOW) to execute a decoder hardware reset. To ensure proper initialization after power is stable,assert RESET for at least 20 ms.
14	VSS	-	Ground for core logic and I/O signals.
15	$\overline{\text{WAIT/DTACK}}$	O	Transfer not complate / data acknowledge. Active LOW to indicate host initiated transfer is not complate.$\overline{\text{WAIT}}$ is asserted after the falling edge of $\overline{\text{CS}}$ and reasserted when decoder is ready to complate transfer cycle. Open drain signal, must be pulled-up via 1kW to 3.3 volts. Driven high for 10 ns before tristate.
16	$\overline{\text{INT}}$	O	Host interrupt. Open drain signal, must be pulled-up via 4.7kW to 3.3 volts. Driven high for 10 ns before tristate.
17	VDD-3.3	-	3.3-V supply voltage for I/O signals.
18	NC	O	No Connection
19	VSS	-	Ground for core logic and I/O signals.
20	NC	O	No Connection
21	PIO11	I/O	Programmable I/O pins. Input mode after reset
22	PIO12		
23	PIO13		
24	PIO14		
25	PIO15		
26	PIO16		
27	VDD-3.3	-	3.3-V supply voltage for I/O signals.
28	PIO17	I/O	Programmable I/O pins. Input mode after reset
29	VSS	-	Ground for core logic and I/O signals.
30	PIO18	I/O	Programmable I/O pins. Input mode after reset
31	PIO19	I/O	Programmable I/O pins. Output mode after reset
32	PIO20		
33	PIO21		
34	PIO22		
35	PIO23		
36	VDD-3.3	-	3.3-V supply voltage for I/O signals.
37	PIO24	I/O	Programmable I/O pins. Output mode after reset
38	VSS	-	Ground for core logic and I/O signals.
39	PIO25	I/O	Programmable I/O pins. Output mode after reset
40	VDD-2.5	-	2.5-V supply voltage for core logic.
41	PIO26	I/O	Programmable I/O pins. Output mode after reset
42	VSS	-	Ground for core logic and I/O signals.

ZIVA3-PEO (2/5)

Pin No.	Symbol	I/O	Function
44 45 46	PIO28 PIO29 PIO30	I/O	Programmable I/O pins. Output mode after reset
47	VDD-3.3	-	3.3-V supply voltage for I/O signals.
48	PIO31	I/O	Programmable I/O pins. Output mode after reset
49	VSS	-	Ground for core logic and I/O signals.
50 51	NC	O	No Connection
52	PIO1	I/O	Programmable I/O pins. Input mode after reset
53	MDATA15	I/O	Memory data
54	MDATA0	I/O	Memory data
55	VDD-3.3	-	3.3-V supply voltage for I/O signals.
56	MDATA14	I/O	Memory data.
57	VSS	-	Ground for core logic and I/O signals.
58 59 60	MDATA1 MDATA13 MDATA2	I/O	Memory data.
61	VDD-3.3	-	3.3-V supply voltage for I/O signals.
62	MDATA12	I/O	Memory data.
63	VSS	-	Ground for core logic and I/O signals.
64	MDATA3	I/O	Memory data.
65	VDD-2.5	-	2.5-V supply voltage for core logic.
66	MDATA11	I/O	Memory data.
67	VSS	-	Ground for core logic and I/O signals.
68	MDATA4	I/O	Memory data.
69	VDD-3.3	-	3.3-V supply voltage for I/O signals.
70	MDATA10	I/O	Memory data.
71	VSS	-	Ground for core logic and I/O signals.
72 73 74	MDATA5 MDATA9 MDATA6	I/O	Memory data.
75	VDD-3.3	-	3.3-V supply voltage for I/O signals.
76	MDATA8	I/O	Memory data.
77	VSS	-	Ground for core logic and I/O signals.
78	MDATA7	I/O	Memory data.
79	LDQM	O	SDRAM LDQM.
80	UDQM	O	SDRAM UDQM.
81	VDD-3.3	-	3.3-V supply voltage for I/O signals.
82	$\overline{\text{MWE}}$	O	SDRAM write enable. Decoder asserts active LOW to request a write operation to the SDRAM array.
83	VSS	-	Ground for core logic and I/O signals.
84	SD-CLK	O	SDRAM system clock.
85	$\overline{\text{SD-CAS}}$	O	Active LOW SDRAM column address.
86	$\overline{\text{SD-RAS}}$	O	Active LOW SDRAM row address.
87	VDD-3.3	-	3.3-V supply voltage for I/o signals.
88	$\overline{\text{SD-CS1}}$	O	Active LOW SDRAM bank select.
89	VSS	-	Ground for core logic and I/O signals.
90	SD-CS0	O	Active LOW SDRAM bank select.
91	VDD-2.5	-	2.5-V supply voltage for core logic.
92	NC	O	No Connection.
93	VSS	-	Ground for core logic and I/O signals.
94	NC	O	No Connection.
95	VDD-3.3	-	3.3-V supply voltage for I/O signals.
96	MADDR9	O	Memory address.
97	VSS	-	Ground for core logic and I/O signals.
98	MADDR11	O	Memory address.

ZIVA3-PEO (3/5)

Pin No.	Symbol	I/O	Function
99	MADDR8	O	Memory address.
100	MADDR10		
101	VDD-3.3	-	3.3-V supply voltage for I/O signals.
102	MADDR7	O	Memory address.
103	VSS	-	Ground for core logic and I/O signals.
104	MADDR0	O	Memory address.
105	MADDR6		
106	MADDR1		
107	VDD-3.3	-	3.3-V supply voltage for I/O signals.
108	MADDR5	O	Memory address.
109	VSS	-	Ground for core logic and I/O signals.
110	MADDR2	O	Memory address.
111	MADDR4		
112	MADDR3		
113	VDD-3.3	-	3.3-V supply voltage for I/O signals.
114	NC	O	No Connection
115	VSS	-	Ground for core logic and I/O signals.
116	NC	O	No Connection
117	VDD-2.5	-	2.5-V supply voltage for core logic.
118	NC	O	No Connection
119	VSS	-	Ground for core logic and I/O signals.
120	NC	O	No Connection
121			
122			
123	VDD-3.3	-	3.3-V supply voltage for I/O signals.
124	NC	O	No Connection
125	VSS	-	Ground for core logic and I/O signals.
126	NC	O	No Connection
127			
128	RESERVED	O	Open drain signal, must be pulled-up via 4.7kW to 3.3 volts.
129	PIO2	I/O	Programmable I/O pins. Input mode after reset.
130	NC	O	No Connection
131	RESERVED	I	Tie to VSS or VDD-3.3
132			
133	PIO3	I/O	Programmable I/O pins. Input mode after reset.
134	VDD-3.3	-	3.3-V supply voltage for I/O signals.
135	RESERVED	I	Tie to VSS or VDD-3.3
136	VSS	-	Ground for core logic and I/O signals.
137	RESERVED	I	Tie to VSS or VDD-3.3
138	PIO4	I/O	Programmable I/O pins. Input mode after reset.
139	RESERVED	I	Tie to VSS or VDD-3.3
140			
141	PIO5	I/O	Programmable I/O pins.Input mode after reset.
142	VDATA0	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
143	VDATA1		
144	VDD-2.5	-	2.5-V supply voltage for core logic.
145	VDATA2	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA
146	VSS	-	Ground for core logic and I/O signals.
147	PIO6	I/O	Programmable I/O pins. Input mode after reset.
148	VDATA3	O	Video data bus. Byte serial CbYCrY data synchronous with VCLK. At power-up, the decoder does not drive VDATA. During boot-up, the decoder uses configuration parameters to drive or 3-state VDATA

ZIVA3-PEO (4/5)

Pin No.	Symbol	I/O	Function
149	VDD-3.3	-	3.3-V supply voltage for I/O signals.
150	VDATA4	O	Video data buses for byte sequential CbYCrY data. The decoder does not run VDATA during the power up procedure. However, during booting the decoder uses operational configuration parameters or 3-state VDATA.
151	VSS	-	Ground for core logic and I/O signals.
152	VDATA5	O	Video data buses for byte sequential CbYCrY data. The decoder does not run VDATA during the power up procedure. However, during booting the decoder uses operational configuration parameters or 3-state VDATA.
153	PIO7	I/O	Programmable I/O pin. Input mode after resetting.
154 155	VDATA6 VDATA7	O	Video data buses for byte sequential CbYCrY data. The decoder does not run VDATA during the power up procedure. However, during booting the decoder uses operational configuration parameters or 3-state VDATA.
156	PIO8	I/O	Programmable I/O.
157	$\overline{\text{HSYNC}}$	I/O	pins. Input mode after reset. Horizontal sync. The decoder begins outputting pixel data for a new horizontal line
158	$\overline{\text{VSYNC}}$	I/O	after the falling (active) edge of HSYNC. Vertical sync.Bi-directional, the decoder outputs the top border of a new field on the first HSYNC aftre the falling edge of VSYNC. VSYNC can accept vertical synchronization or top/bottom field notification from an external source.
159	DA-IEC	O	(VSYNC HIGH = bottom field. VSYNC LOW = Top field)
160	VDD-3.3	-	Bistream data in IEC-1937 or PCM data out in IEC-958 format.
161	DA-DATA0	O	3.3-V supply voltage for I/O signals.
162	VSS	-	PCM data out, eight channels. Serial audio samples relative to DA-BCK clock.
163 164 165	DA-DATA1 DA-DATA2 DA-DATA3	O	Ground for core logic and I/O signals. PCM data out, eight channels. Serial audio samples relative to DA-BCK clock.
166	DA-LRCK	O	PCM left-right clock. Identifies the channel for each audio sample. the polarity is
167	DA-BCK	O	programmable. PCM bit clock. Divided by 8 from DA-XCK can be either 48 or 32 times the sampling
168	VDD-2.5	-	clock.
169	DA-XCK	I/O	2.5-V supply voltage for core logic. Audio master frequency clock. Used to generate DA-BCK and DA-LRCK. DA-XCK can
170	VSS	-	be eigher 384 or 256 times the sampling frequency.
171	DAI-DATA	I	Ground for core logic and I/O signals.
172	DAI-LRCK	I	PCM input data. two channels. Serial audio samples relative to DAI-BCK clock.
173	DAI-BCK	I	PCM input left-right clock.
174	PIO9	I/O	PCM input bit clock.
175	CLKSEL	I	Programmable I/O pins. Input mode after reset.
176	A-VDD	-	Clock Select: Internal = VDD, External = VSS
177	VCLK	I	3.3-V analog supply voltage.
178	SYSCLK	I	Video clock. Clocks out data on input. VDATA7.Clock is typically 27 MHz. System clock.Decoder requires external 27 MHz TTL oscilator.
179	A-VSS	-	Drive with the same 27-MHz as VCK.
180	DVD-DATA0 /CD-DATA	I	Analog ground for PLL Serial CD data. This pin is shared with DVD compressed data DVD-DATA0.
181	VDD-3.3	-	
182	DVD-DATA1 /CD-LRCK	I	3.3-V supply voltage for I/O signals. Programmable polarity 16-bit word synchronization to the decoder
183	VSS	-	(right channel HIGH). This pin is shared with DVD compressed data DVD-DATA1.
184	DVD-DATA2 /CD-BCK	I	Ground for core logic and I/O signals. CD bit clock. Decoder accept multiple BCK rates. This pin is shared with DVD
185	DVD-DATA3 /CD-C2PO	I	compressed data DVD-DATA2. Asserted HIGH indicates a corrupted byte.Decoder keeps the previous valid picture on-screen unit the next valid picture is decoded. This pin is shares with DVD compressed data DVD-DATA3.

ZIVA3-PEO (5/5)

Pin No.	Symbol	I/O	Function
186 187 188 189	DVD-DATA7 /CDG-SCLK DVD-DATA6 /CDG-SOS1 DVD-DATA5 /CDG-VFSY DVD-DATA4 /CDG-SDATA	I	DVD parallel compressed data from DVD DSP. When DVD DSP sends 32-bit words, it must write the MSB first. CDG-SDATA:CD+G (Subcode) Data.Indicates serial subcode data input. CDG-VSFY:CD+G (Subcode)Frame Sync. Indicates frame-start or composite synchronization input. CDG-SOS1:CD+G (Subcode) Block Sync.Indicates block-start synchronization input. CDG-SCLK: CD+G(Subcode)Clock. Indicates subcode data clock input or output.
190	PIO10	I/O	Programmable I/O pins. Input mode after reset.
191	VREQUEST	O	Video request. Decoder asserts VREQUEST to indicate that the video input buffer has available space.Polarity is programmable.
192	VSTROBE	I	Video strobe. Programmable dual mode pulse. Asynchronous and synchronous. In Asynchronous mode, an external source pulses VSTROBE to indicate data is ready for transfer. In synchronous mode VSTROBE clock data.
193	VDD-3.3	-	3.3-V supply voltage for I/O signals.
194	NC	O	No Connection
195	VSS	-	Ground for core logic and I/O signals.
196	V-DACK	I	In synchronous mode, Video data acknowledge. Asserted when DVD data is valid.Polarity is programmable.
197	VDD-2.5	-	2.5-V supply voltage for core logic.
198	RESERVED	I	Tie to VSS or VDD-3.3
199	VSS	-	Ground for core logic and I/O signals.
200	ERROR	I	Error in input data. If ERROR signal is not available from the DSP it must be grounded.
201	HOST8SEL	I	Always Ttie to VDD-3.3
202 203 204	HADDR0 HADDR1 HADDR2	I	Host address bus. 3-bit address bus selects one of eight host interface registers.
205	DTACKSEL	I	Tie HIGH to select $\overline{\text{WAIT}}$ signal, LOW to select $\overline{\text{DTACK}}$ signal (Motorola 68K mode).
206	$\overline{\text{CS}}$	I	Host chip select.Host asserts CS to select the decoder for a read or write operation.The falling edge of this signal triggers the read or write operation.
207	R/$\overline{\text{W}}$	I	Read/write strobe in M mode. write strobe in I mode.Host asserts R/$\overline{\text{W}}$ LOW to select write and LOW to select read.
208	$\overline{\text{RD}}$	I	Read strobe in I mode. Must be held HIGH in M Mode

JVC

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